

**Platform : Haswell + Lynx Point+N16P-GX**

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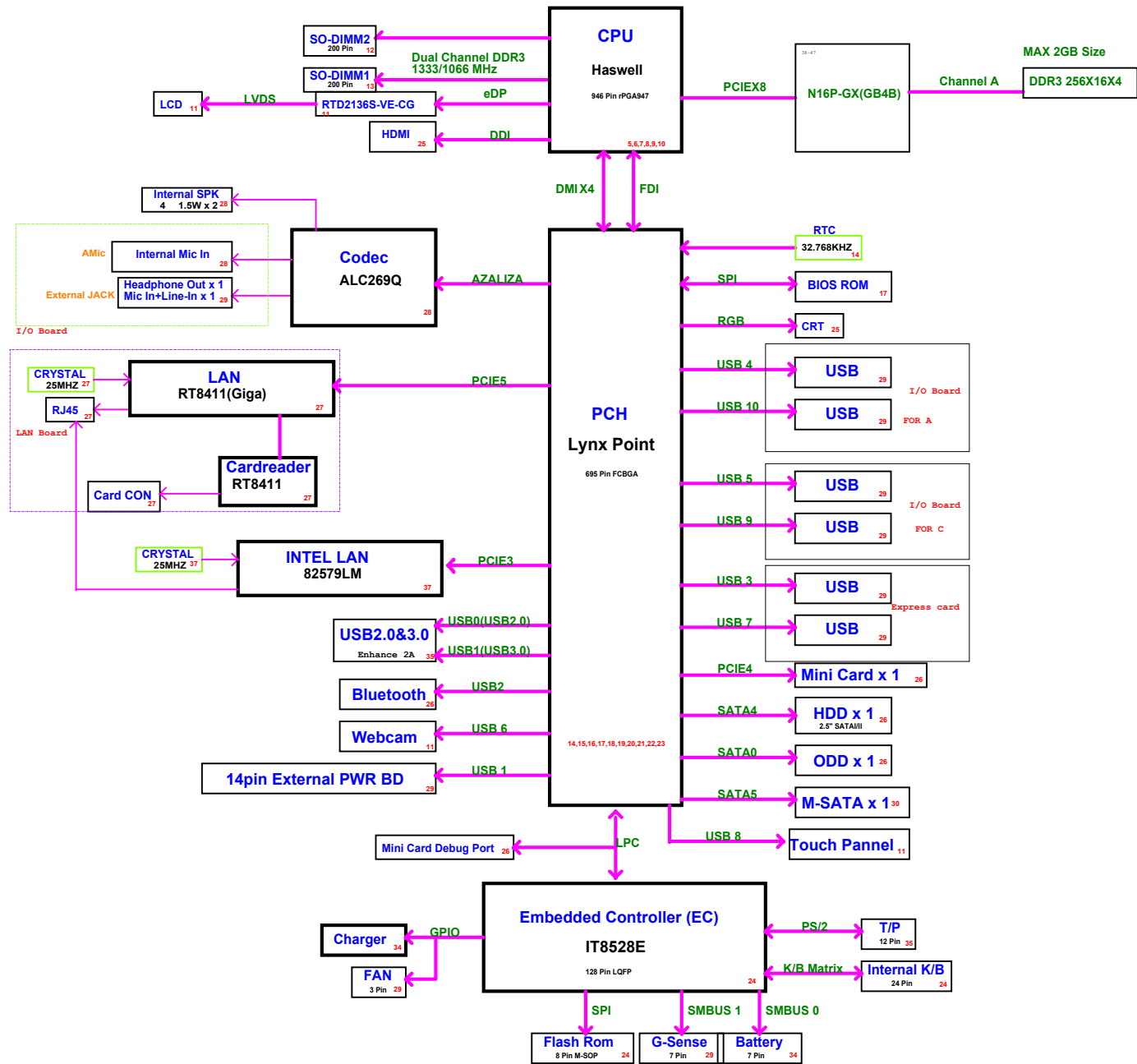
## M/B Schematic Version Change List

[illegible]

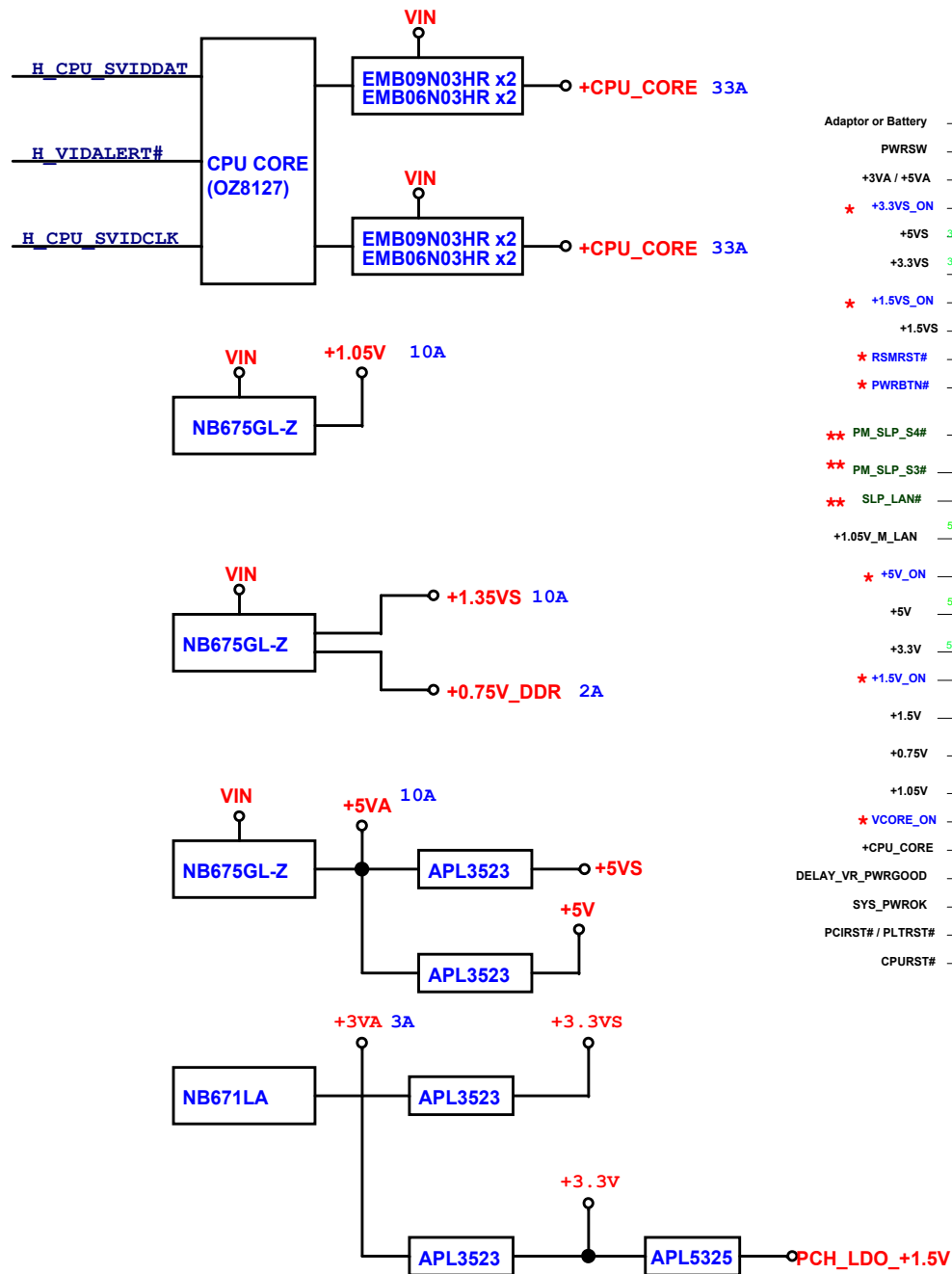
## Daughter Board Schematic Version Change List

[illegible]

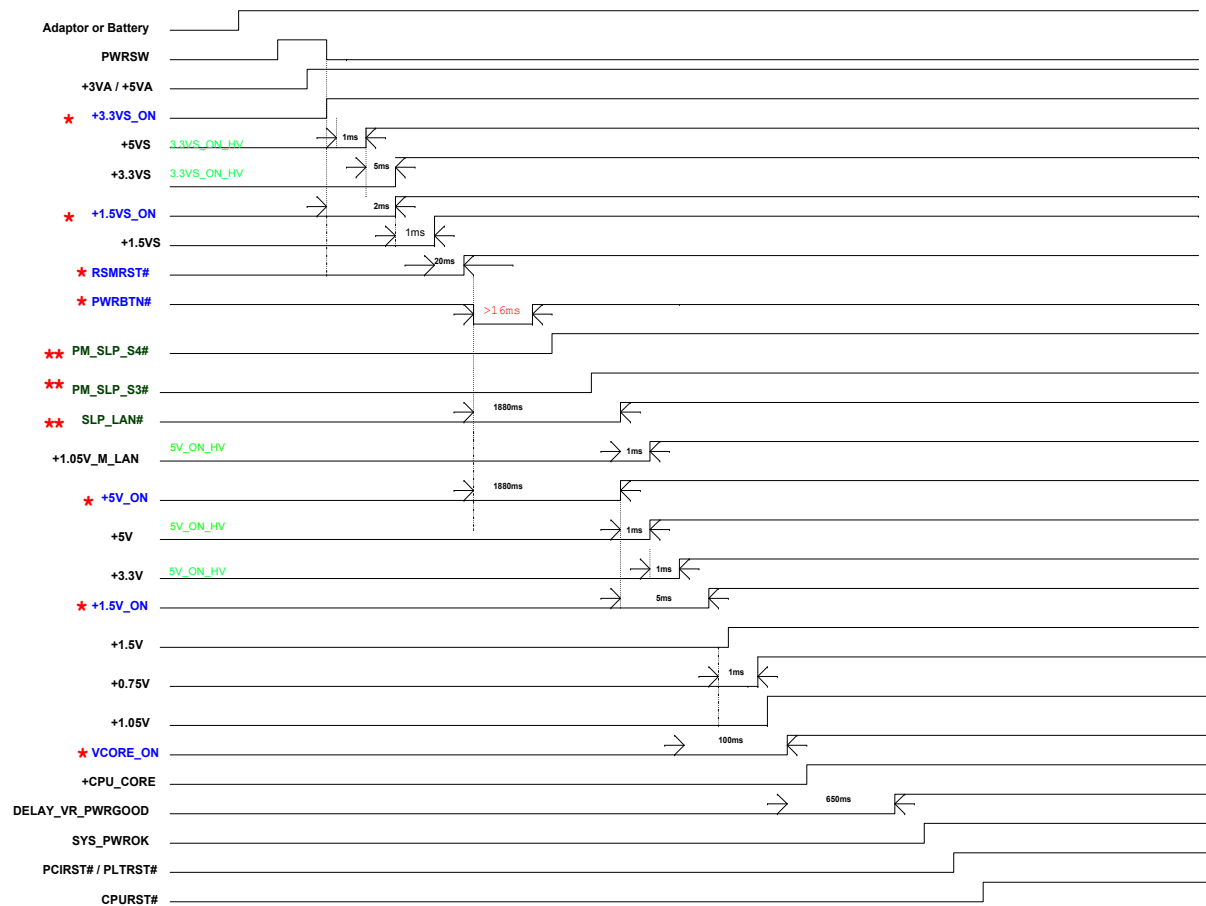
SYSTEM BLOCK DIAGRAM



# POWER BLOCK DIAGRAM

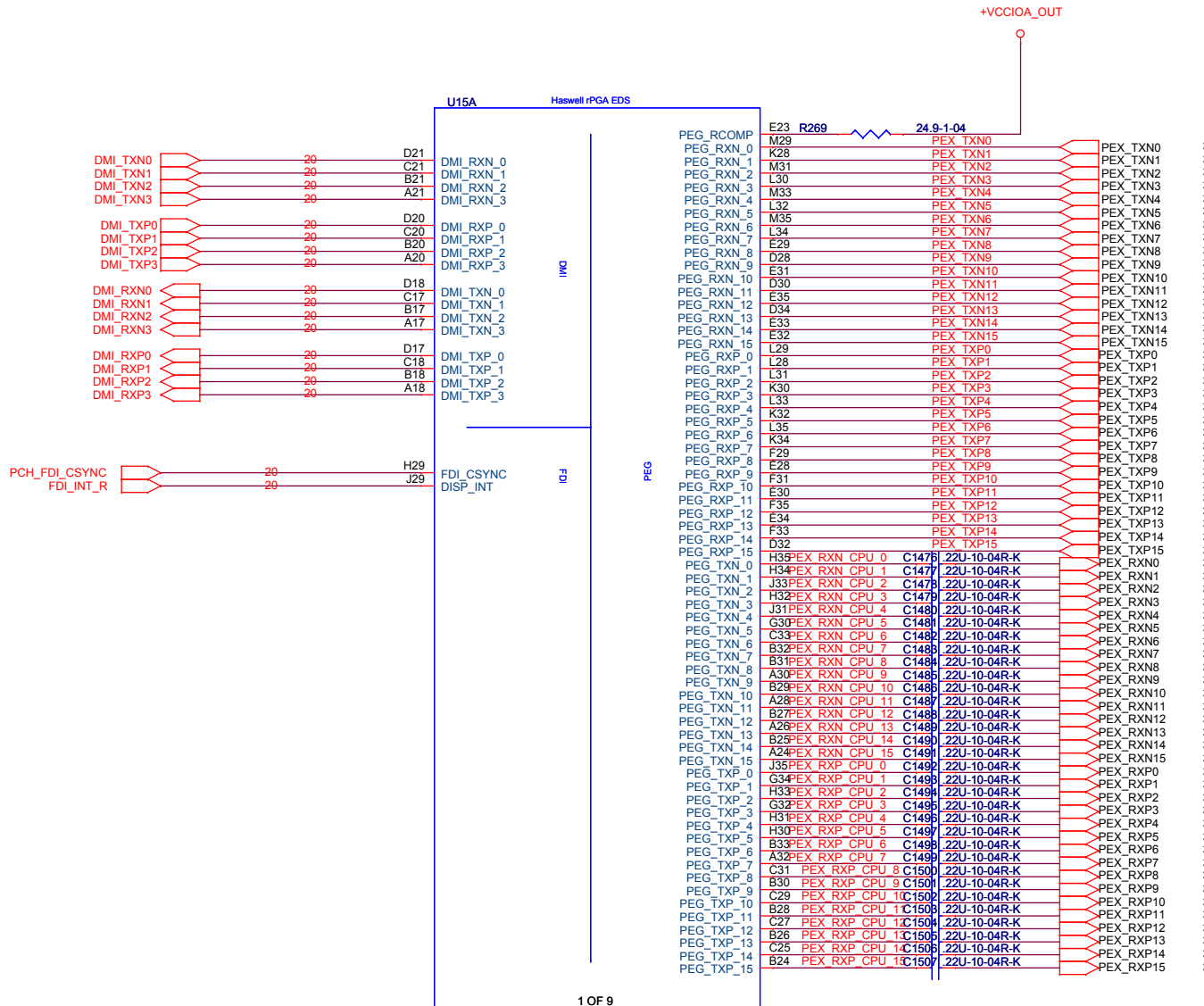


# System Poewr On Sequence



★ EC Control Pin (O/P)  
★★ EC Control Pin (I/P)

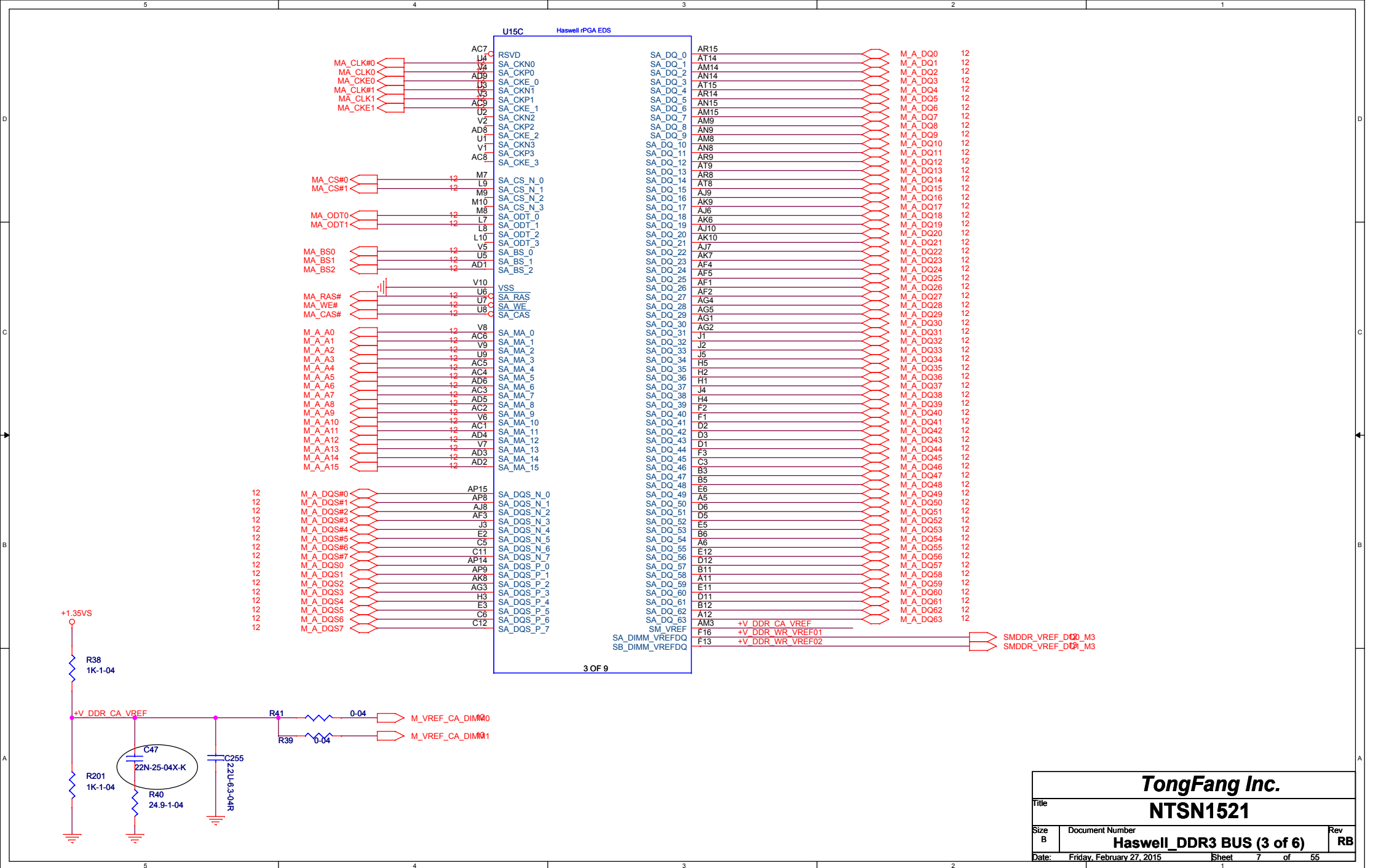


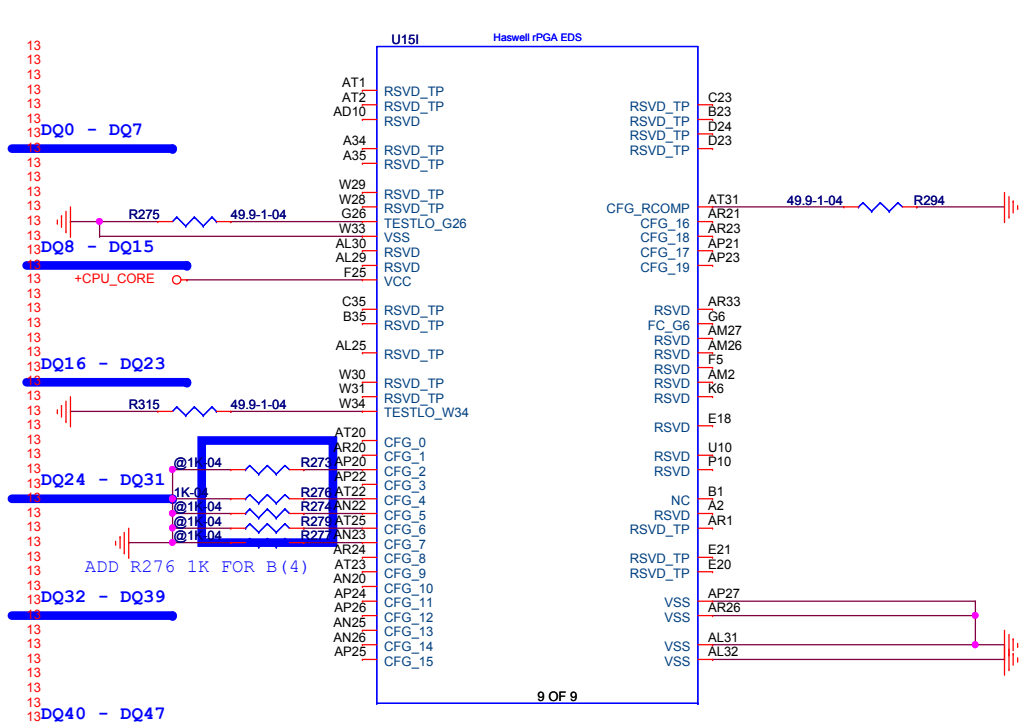
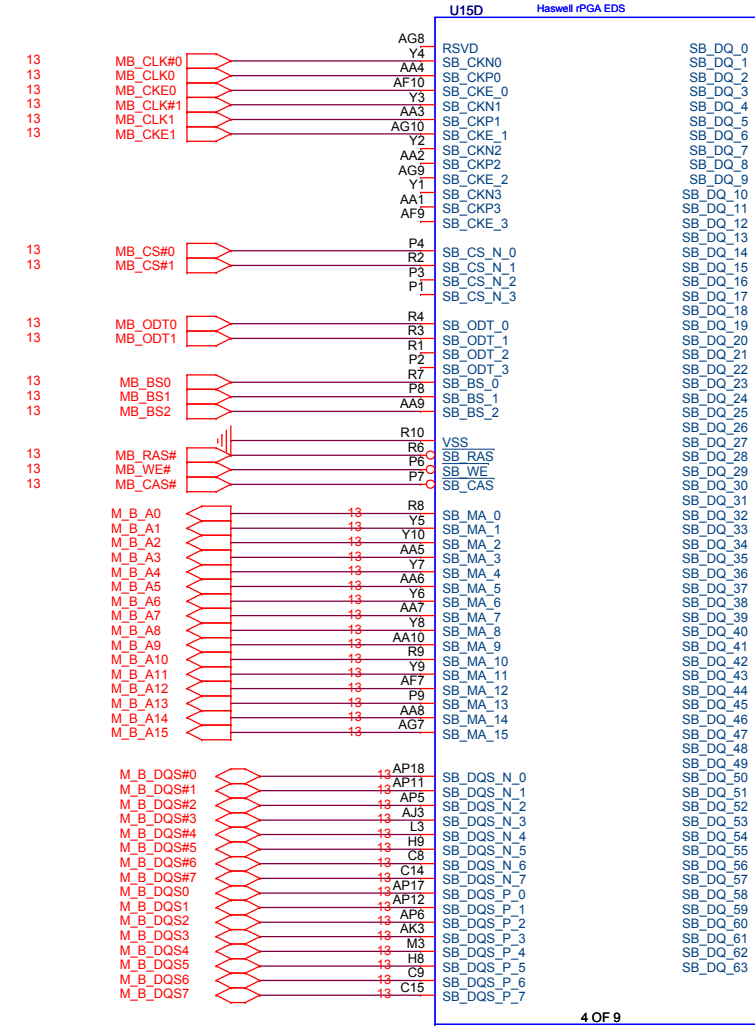


The 16 lanes are associated with root port of device 1  
Function 0 refers to the controller of the x16  
Function 1 refers to the controller of the x8  
Function 2 refers to the controller of the x4

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CFG[4]: eDP enable 1 = Disabled 0 = Enabled

CFG[6:5]

11: (Default) x16 - Device 1 functions 1 and 2 disabled  
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled  
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)  
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

DEFENSIVE PULL DOWN SITE

CFG7 1: (Default) PEG Train immediately following xxRESETB de assertion  
0: PEG Wait for BIOS for training

PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS

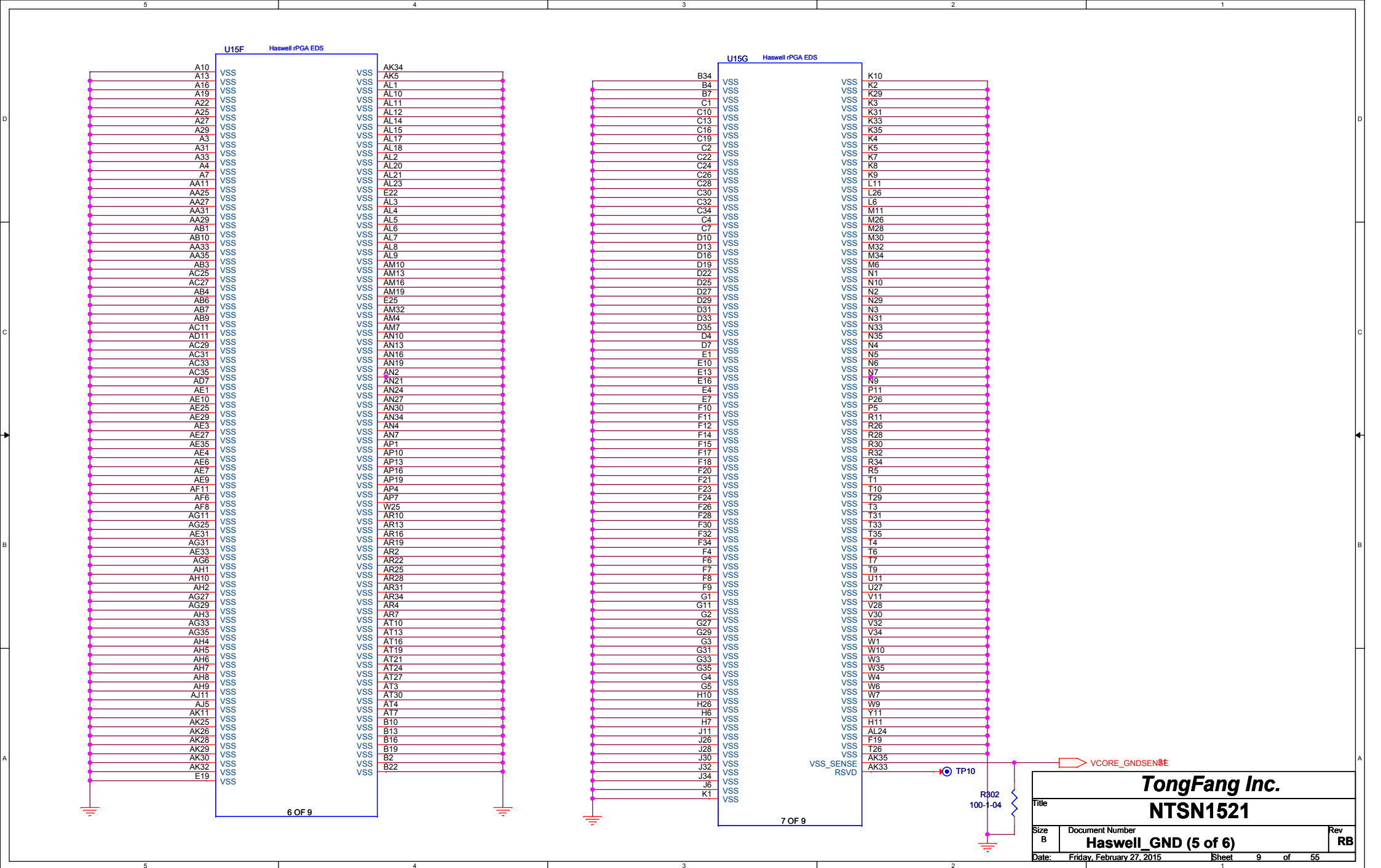
CFG2

1: (DEFAULT)NORMAL OPERATION;  
LANE# DEFINITION MATCHES  
SOCKET PIN MAP DEFINITION  
0: LANE REVERSAL

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NTSN1521

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Haswell\_DDR3 BUS/RSVD (4 of 6)  
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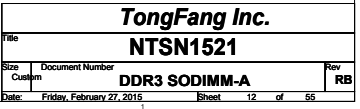




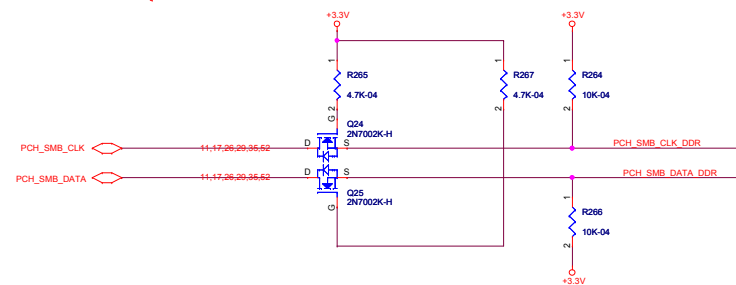
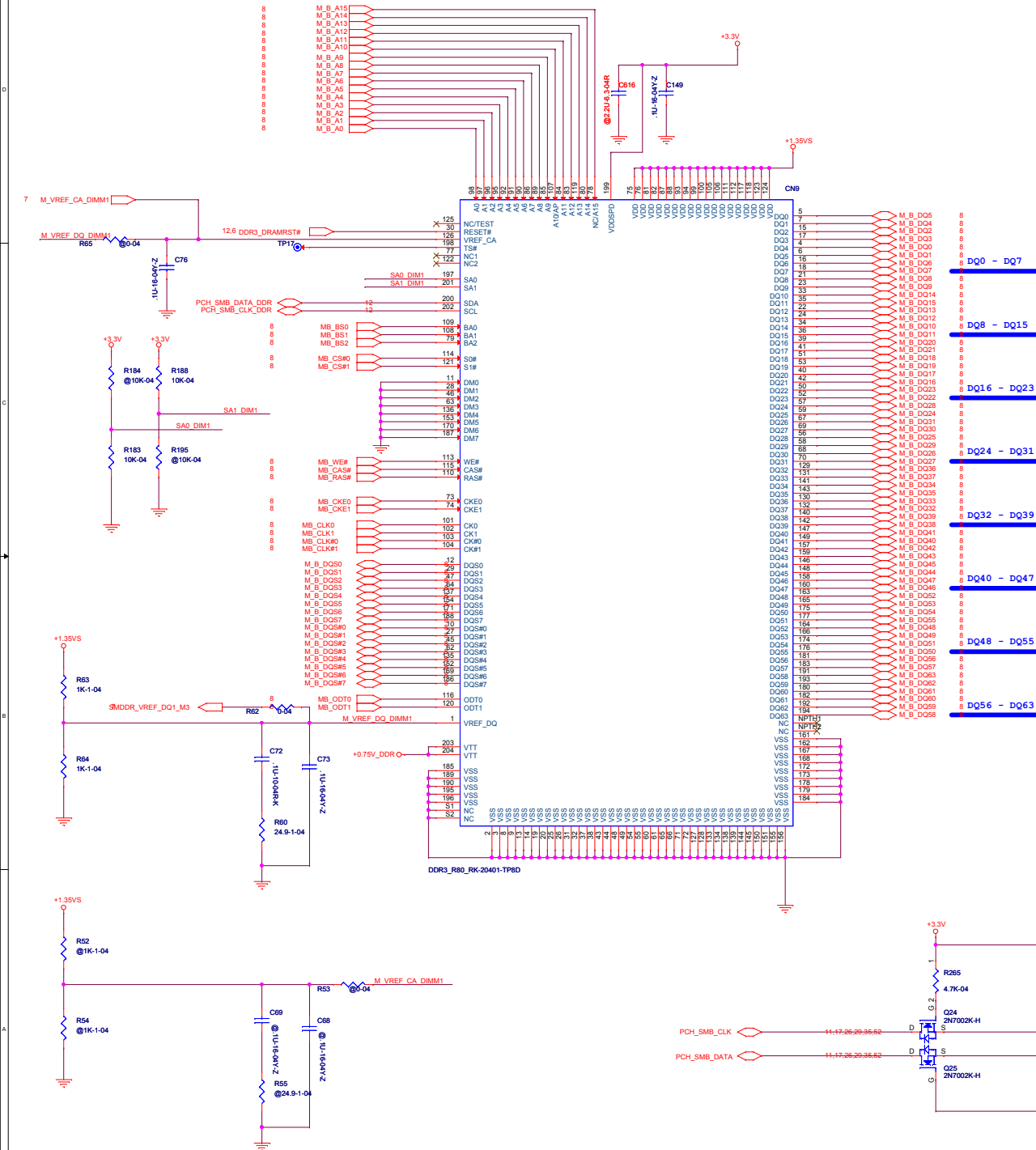
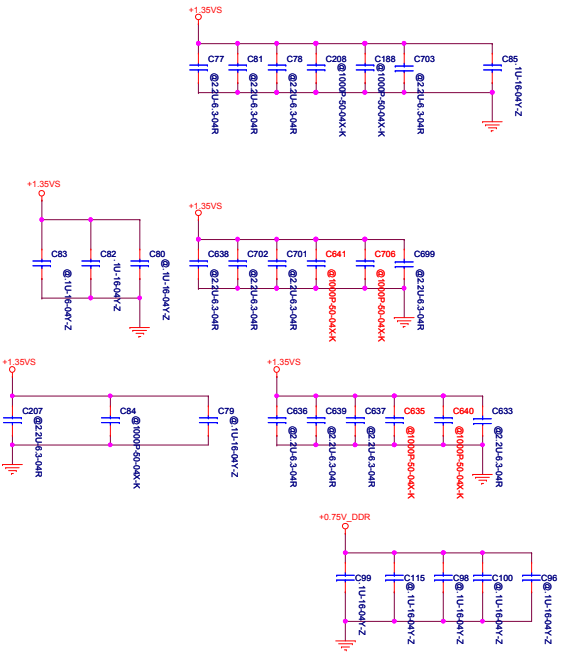
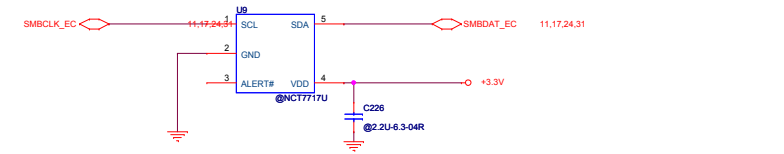
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Title		
Size B	Document Number	Rev
	<b>Haswell_GND (5 of 6)</b>	<b>RB</b>
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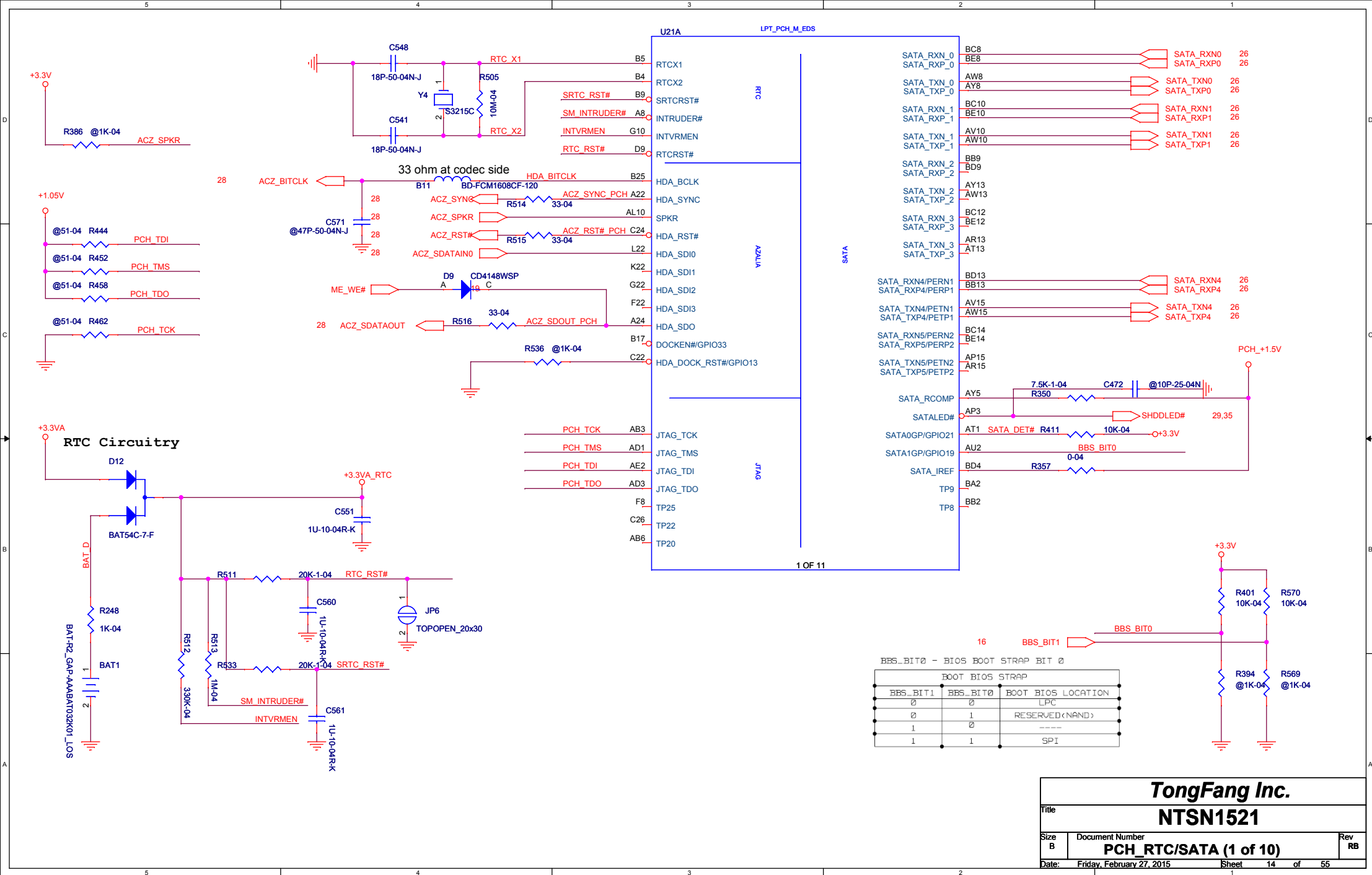




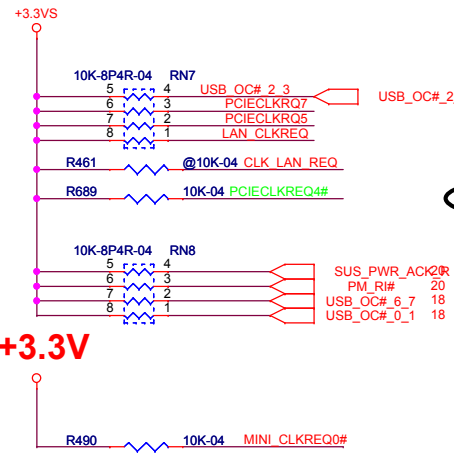


### CPU Thermal Sensor

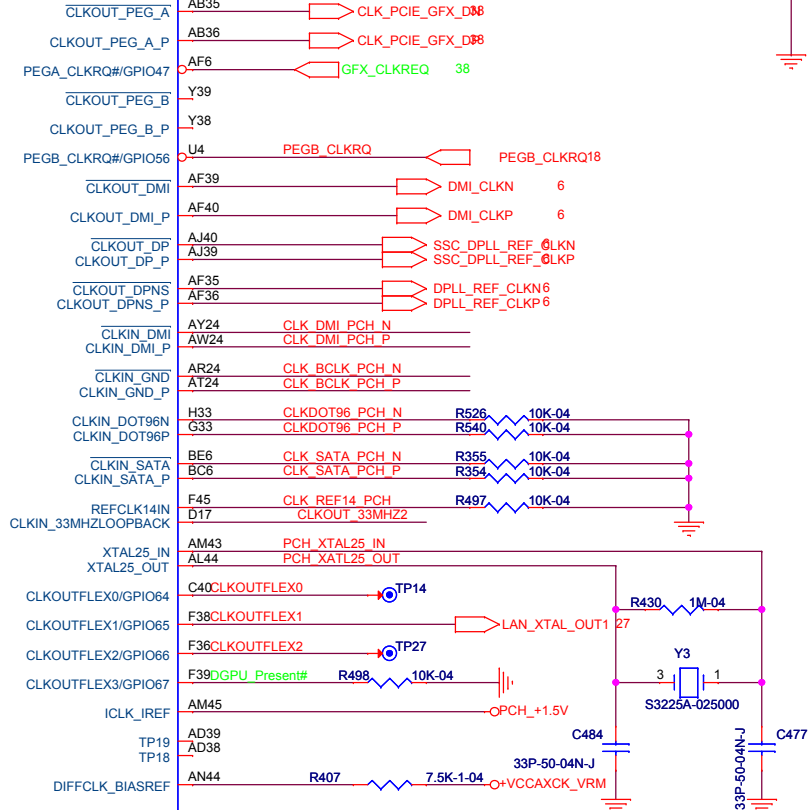
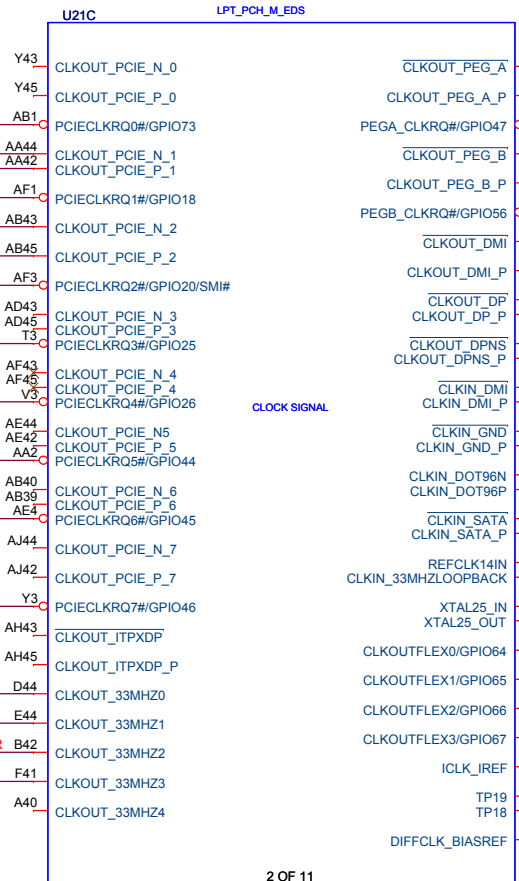
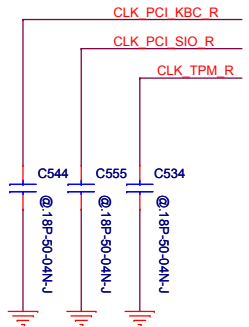
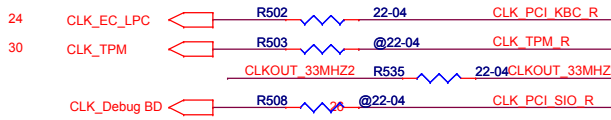




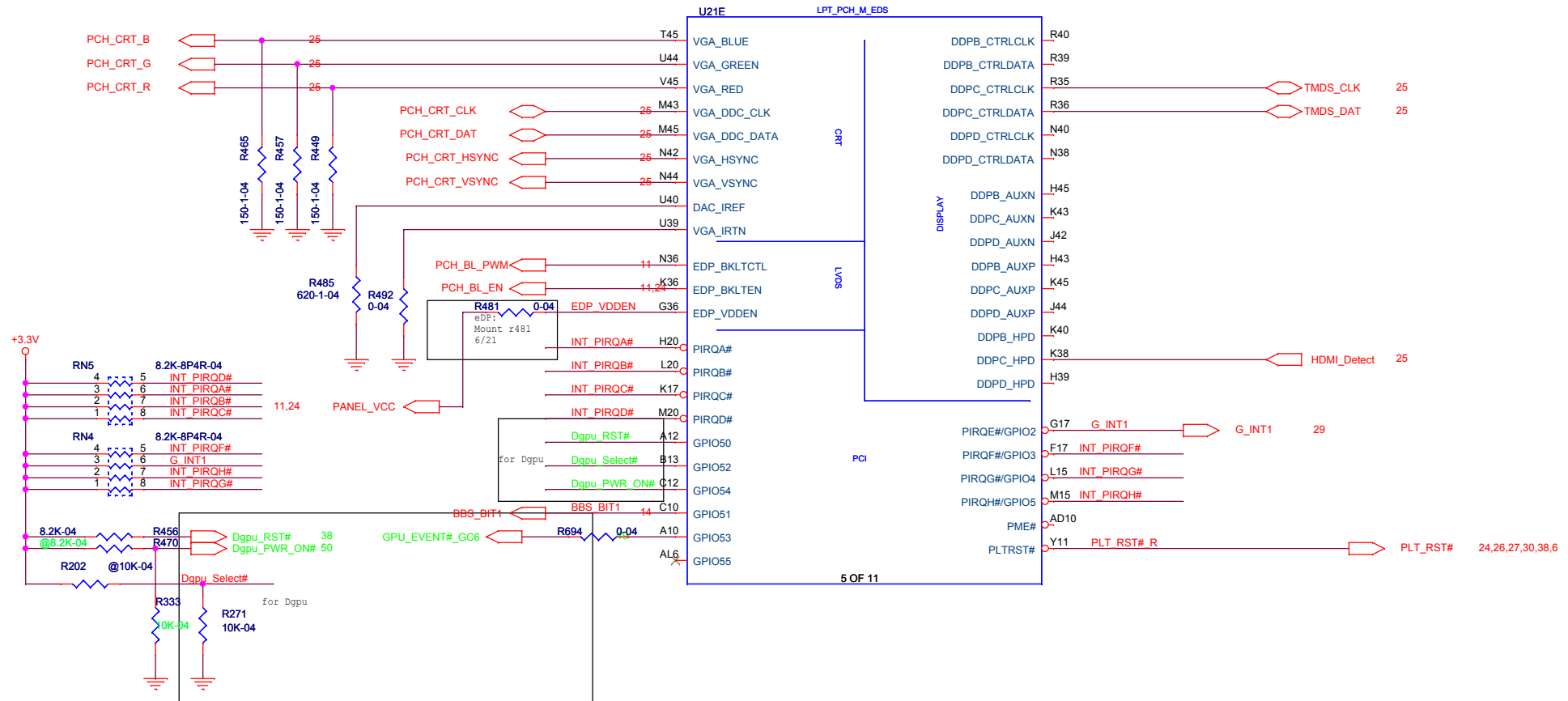
PCIE	Location
PCIE 0	LAN+cardreader
PCIE 1	WLAN
PCIE 2	Express Card
PCIE 3	Express Card
PCIE 4	INTEL LAN
PCIE 6	no use
PCIE 7	no use
PCIE 8	no use



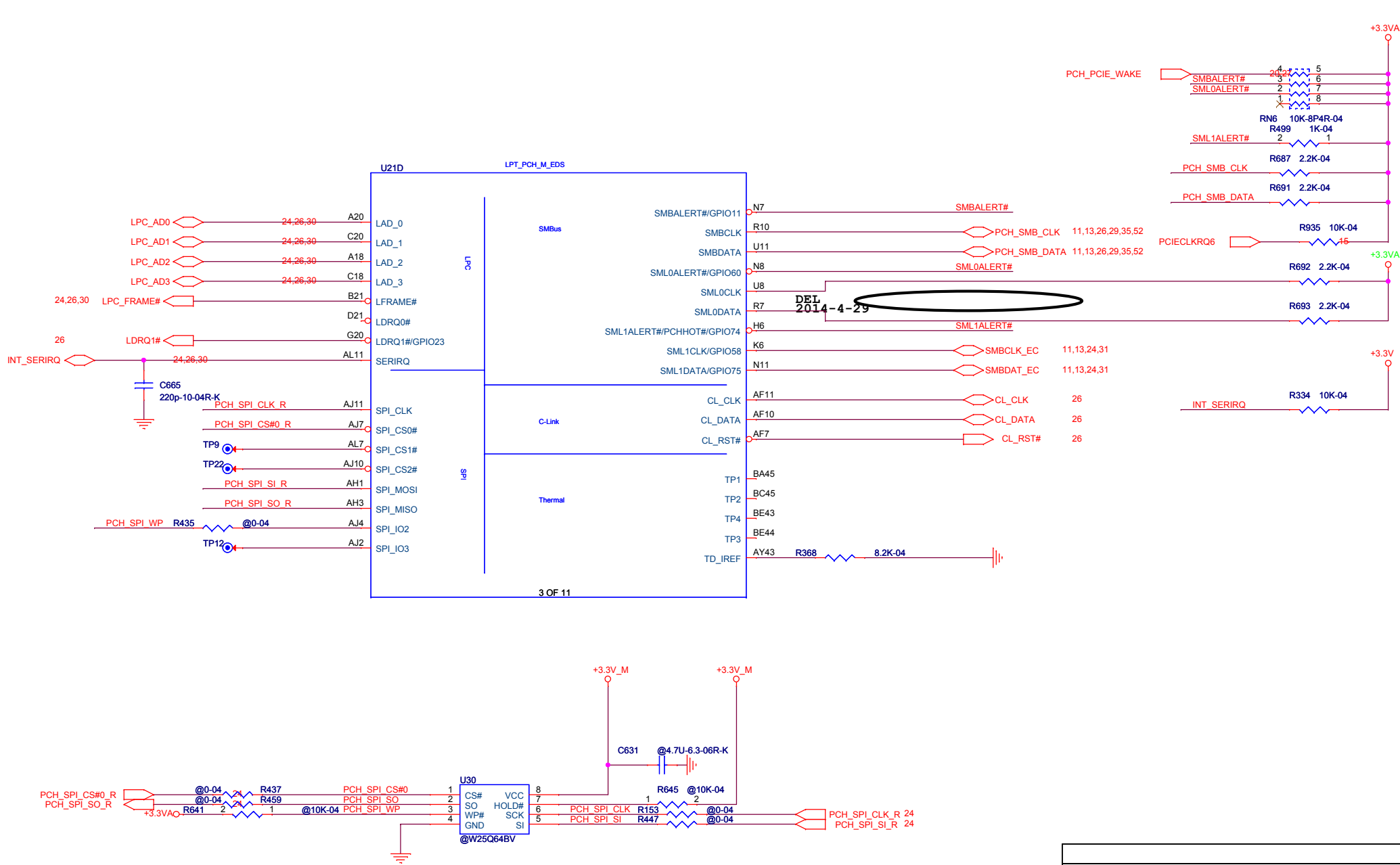
DEL  
2014-4-29



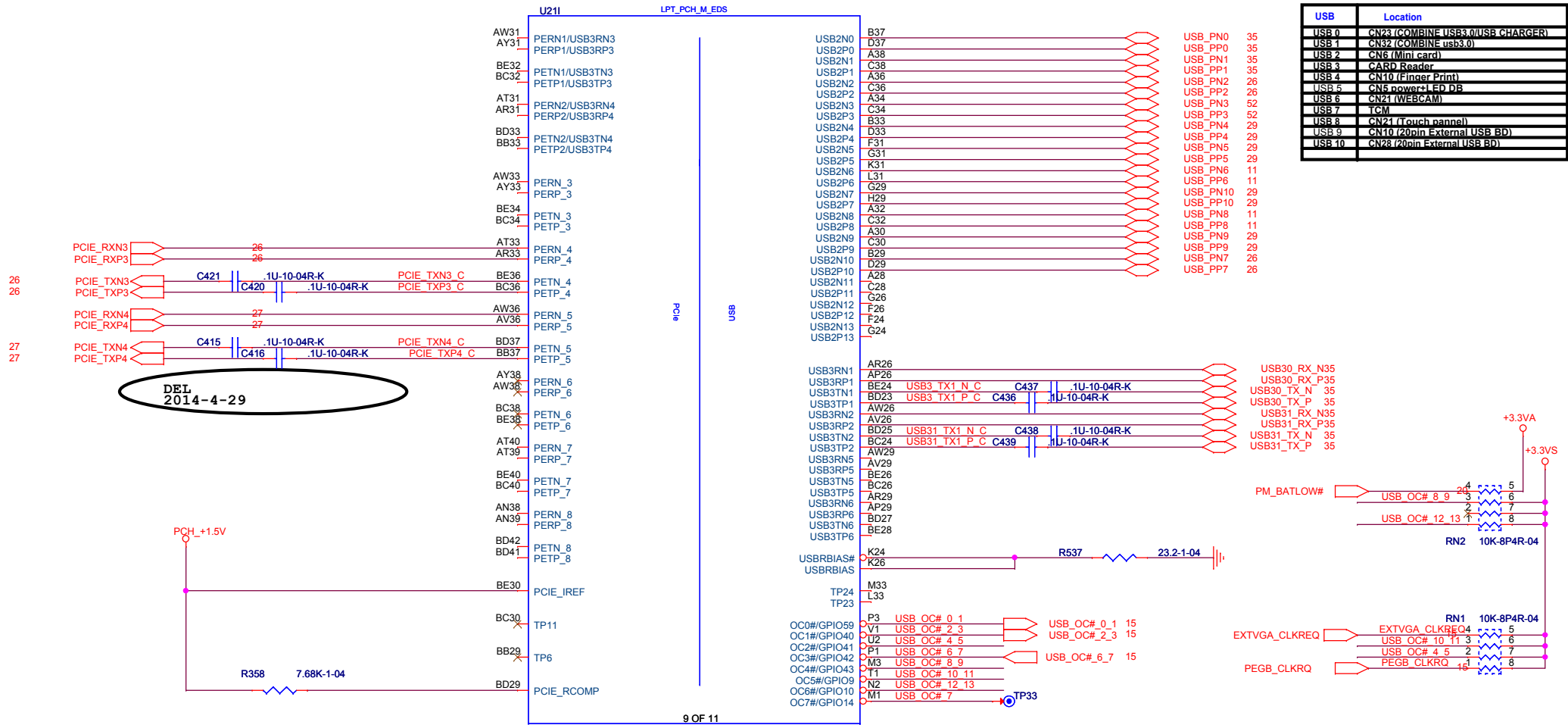
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Title	Document Number	Rev	RB
B	PCH_CLK(2 of 9)		
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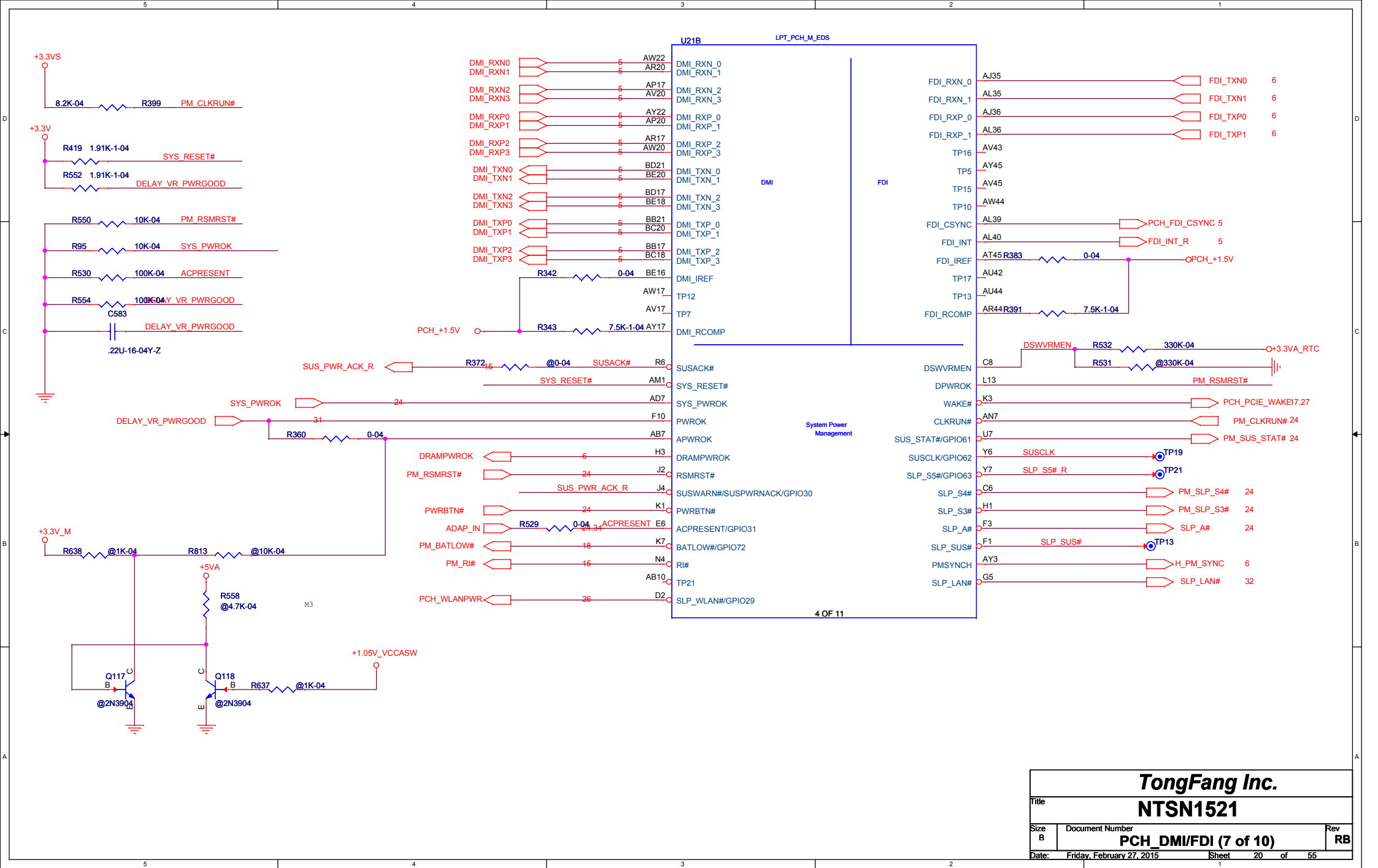
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Size	Document Number		Rev	
B	PCH_SPI/SMB/LAD(4 of 10)		RB	
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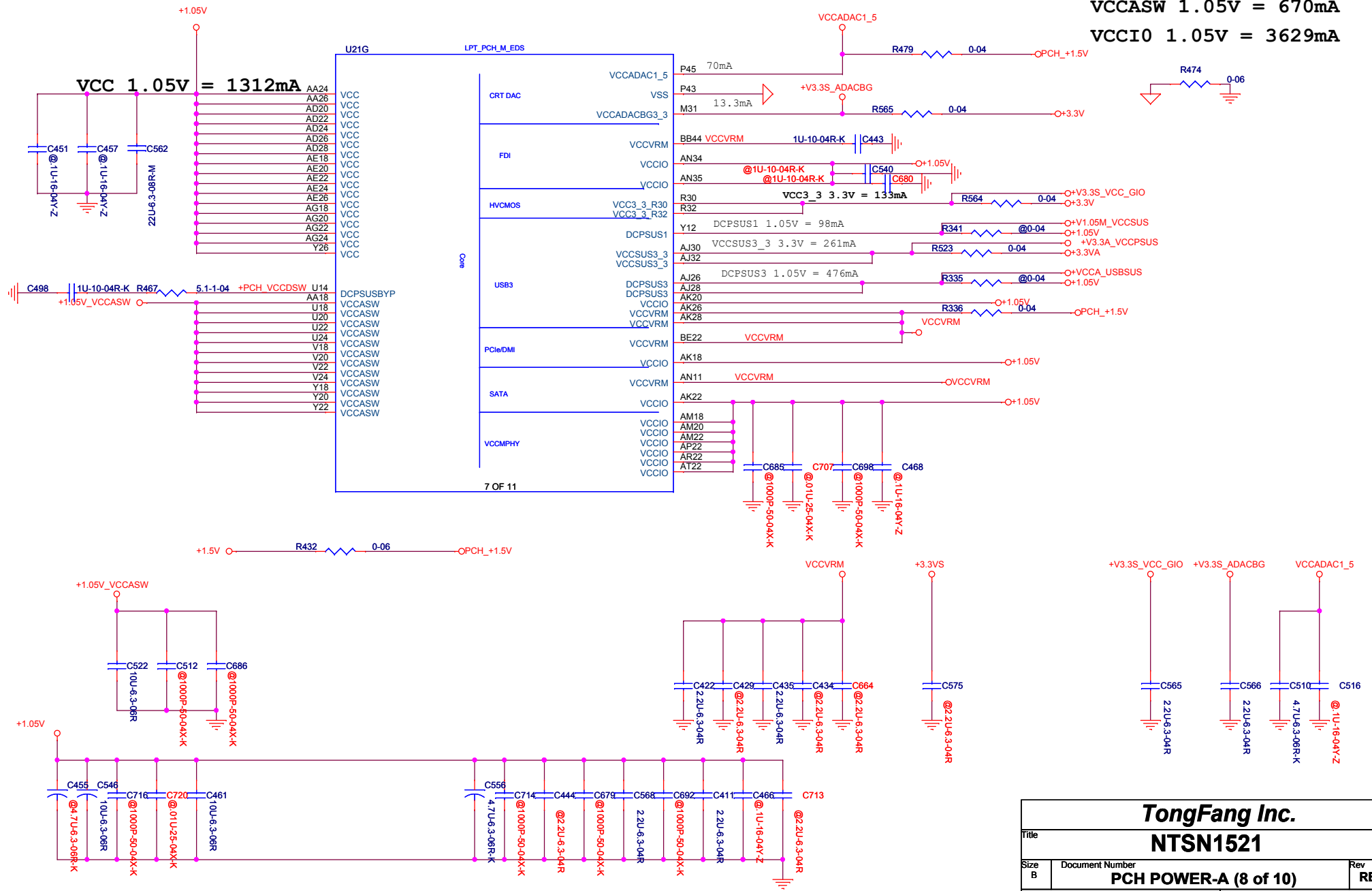
USB	Location
USB 0	CN23 (COMBINE USB3.0/USB CHARGER)
USB 1	CN32 (COMBINE usb3.0)
USB 2	CN6 (Mini card)
USB 3	CARD Reader
USB 4	CN10 (Finger Print)
USB 5	CN5 power+LED DB
USB 6	CN21 (WEBCAM)
USB 7	TCM
USB 8	CN21 (Touch panel)
USB 9	CN10 (20pin External USB BD)
USB 10	CN28 (20pin External USB BD)

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	PCH_PCIE/USB (5 of 10)	RB	
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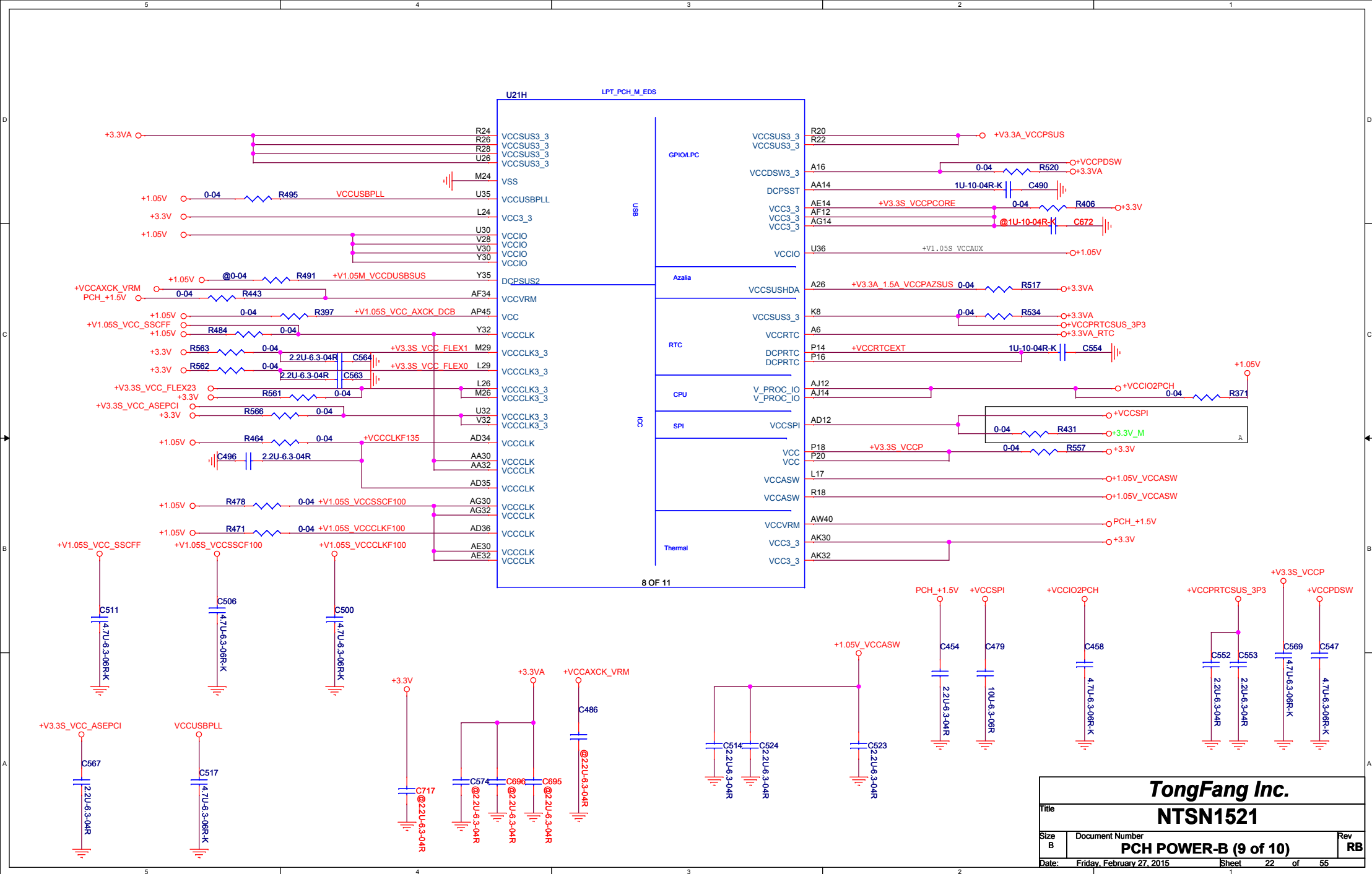


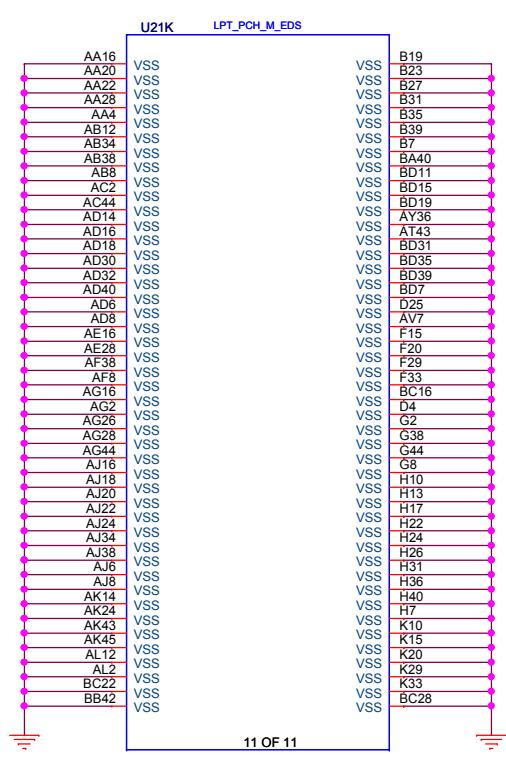
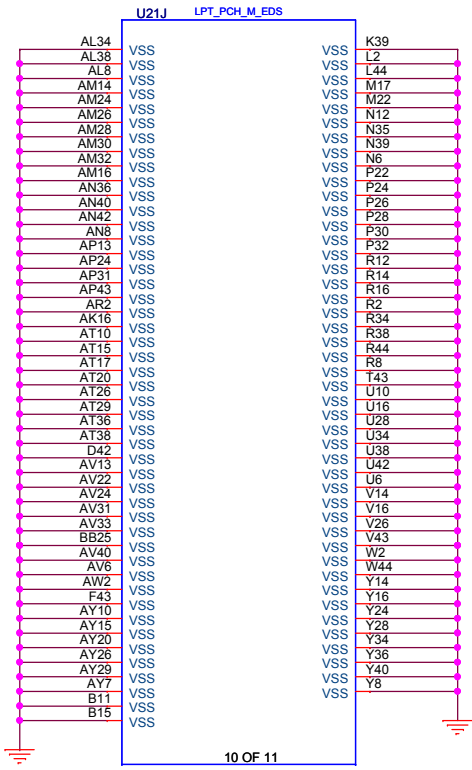


VCCRAM 1.5V = 183mA  
VCCASW 1.05V = 670mA  
VCCIO 1.05V = 3629mA



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B	PCH POWER-A (8 of 10)	RB	
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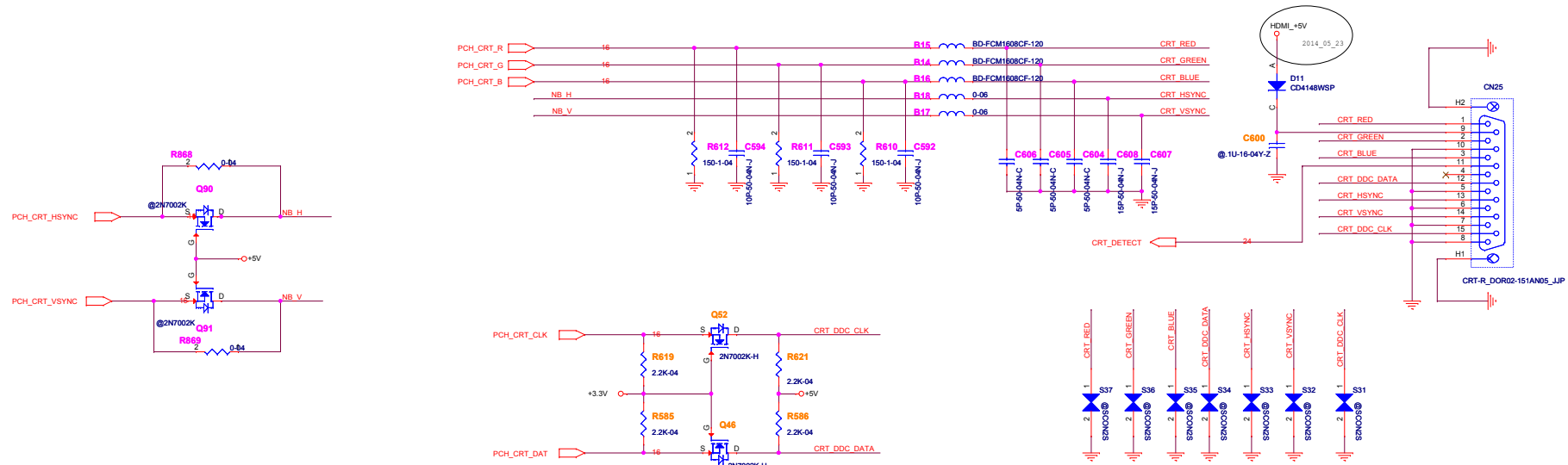




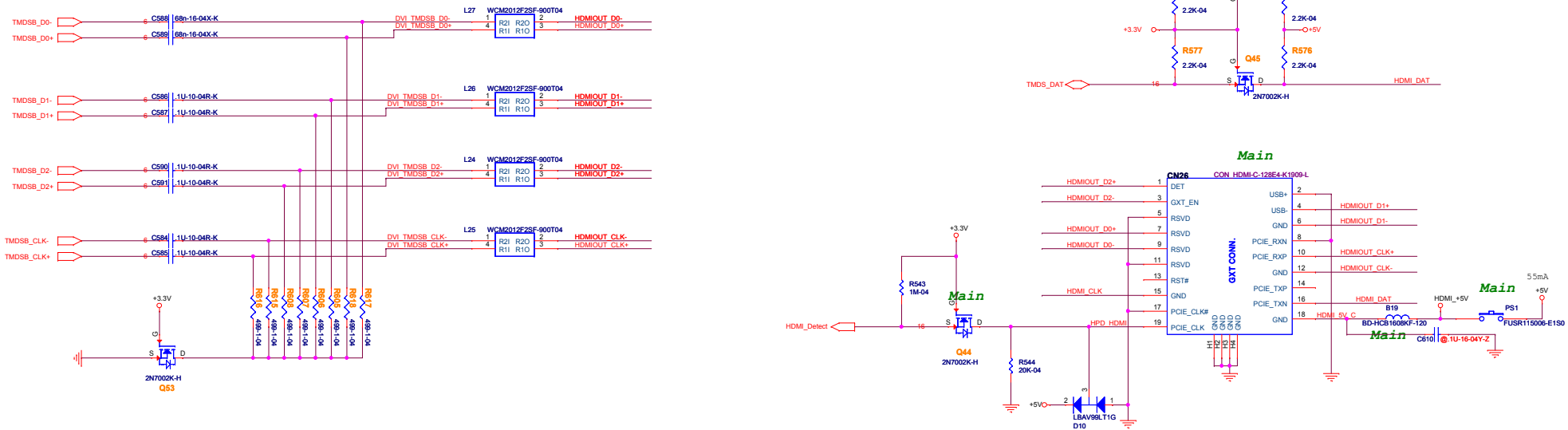




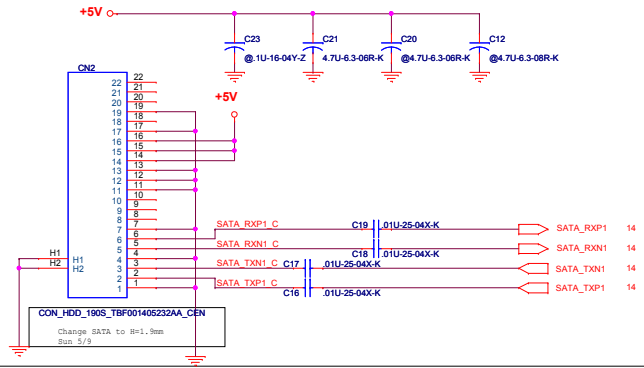
## CRT CONN



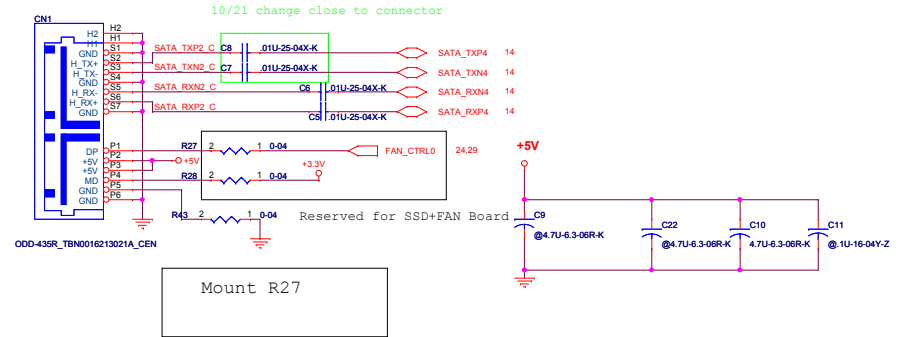
## HDMI CONN



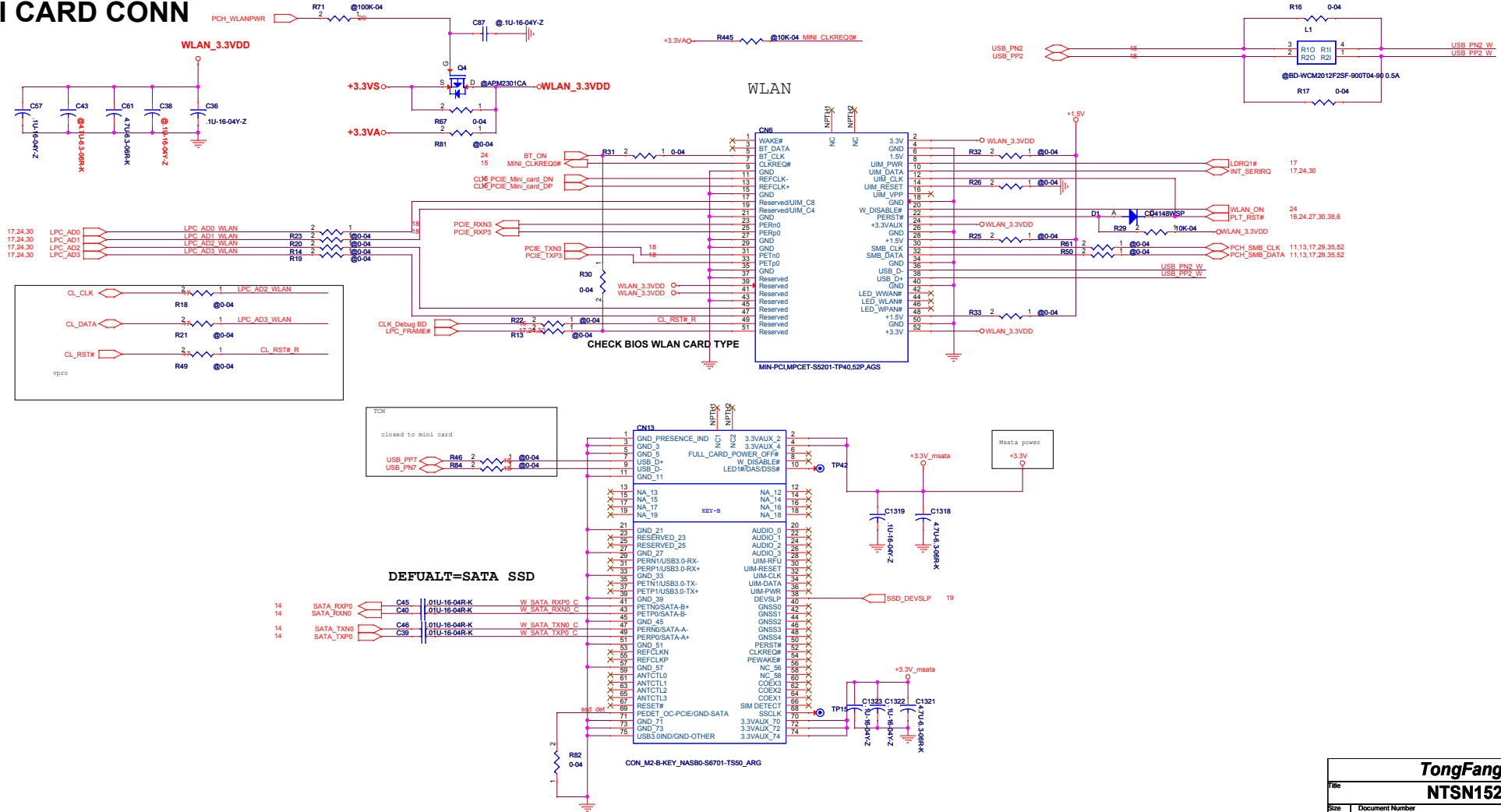
## SATA-HDD

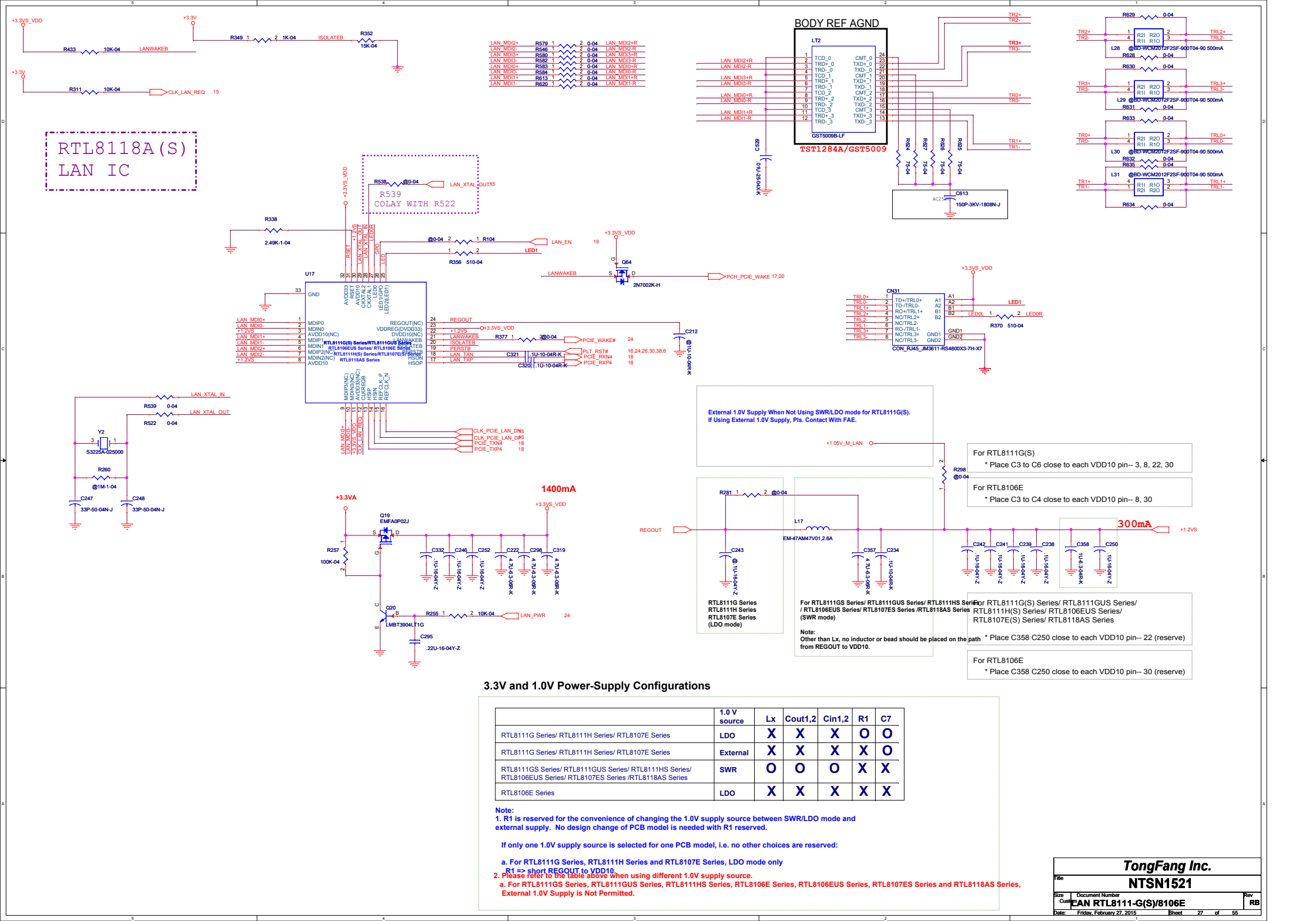


## CD-ROM

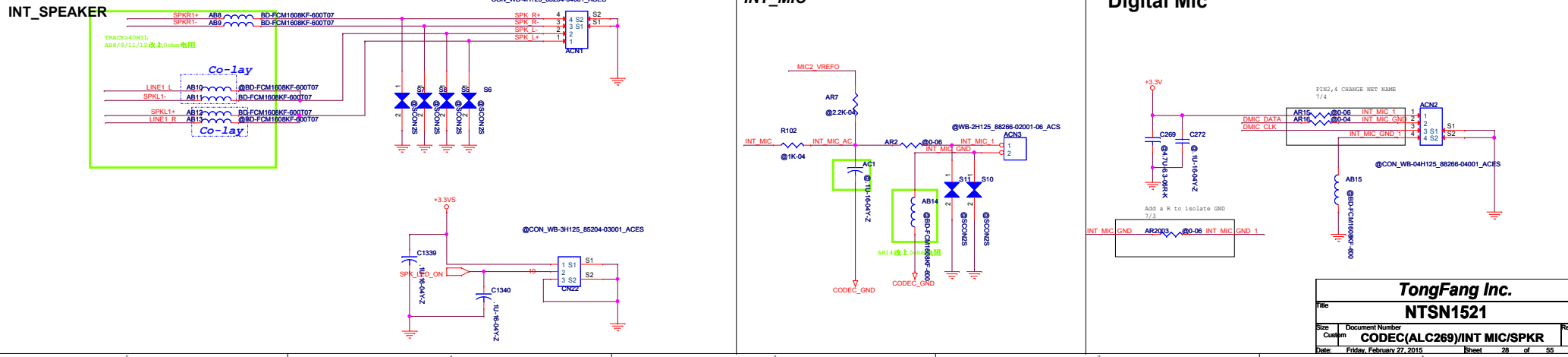


## MINI CARD CONN

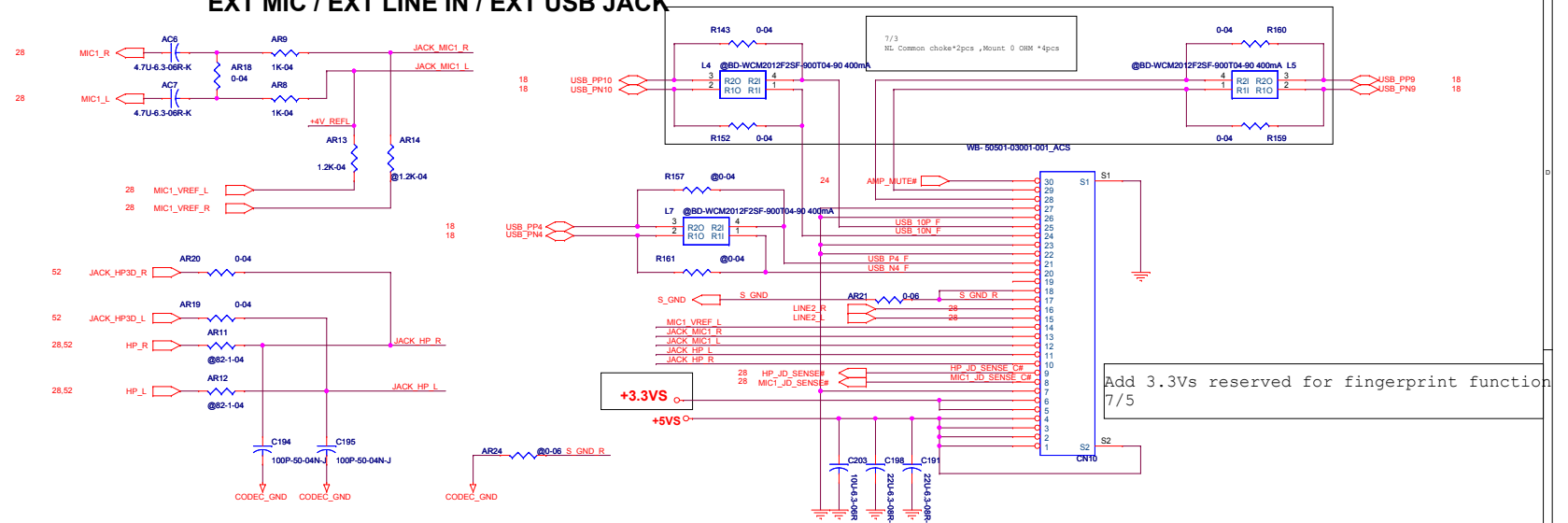




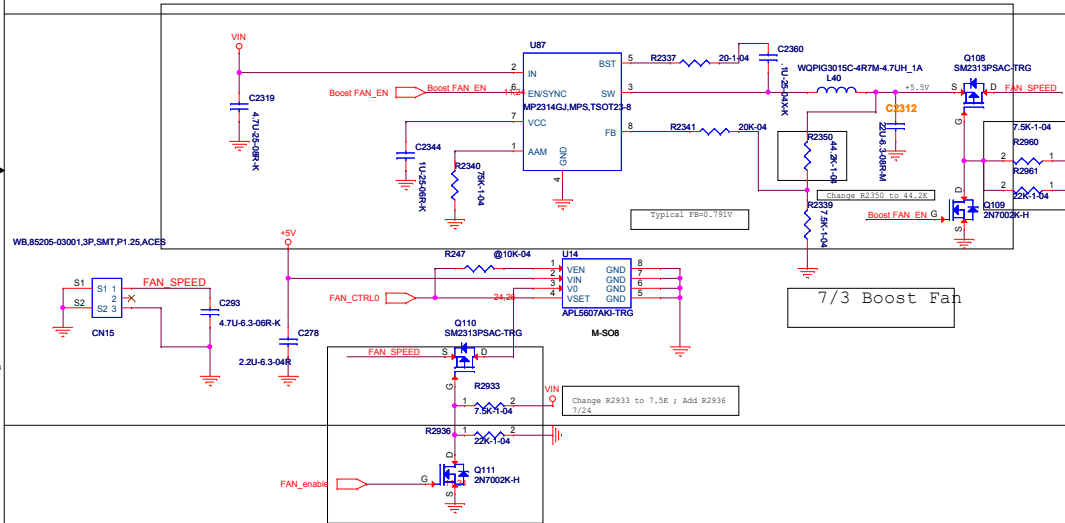
**AMP VDD**



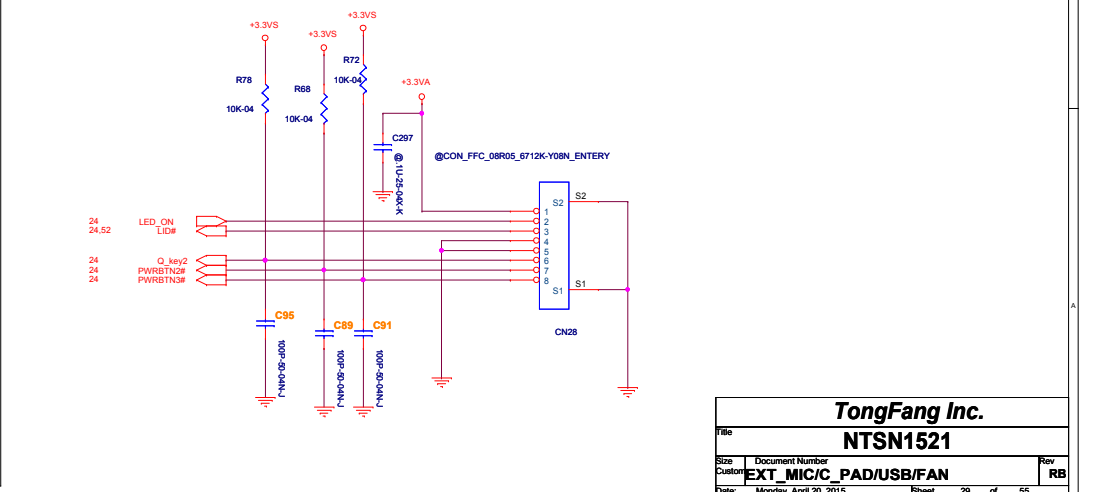
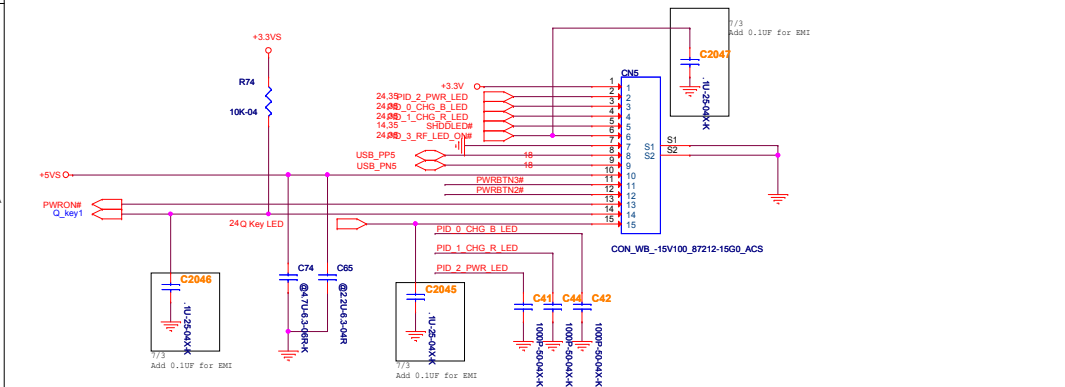
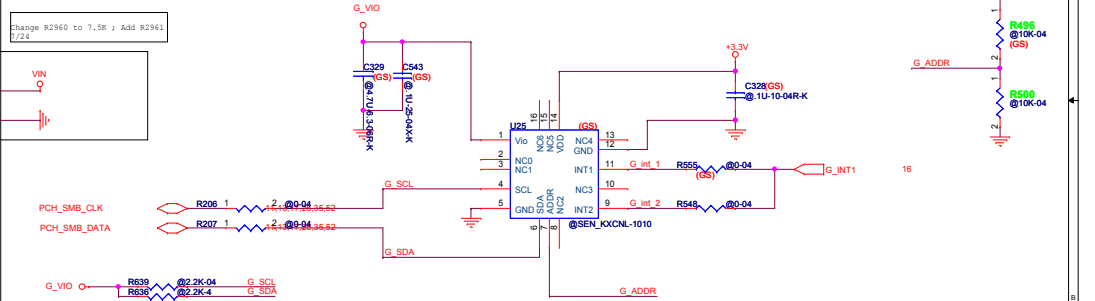
# EXT MIC / EXT LINE IN / EXT USB JACK



## FAN CONTROLLER



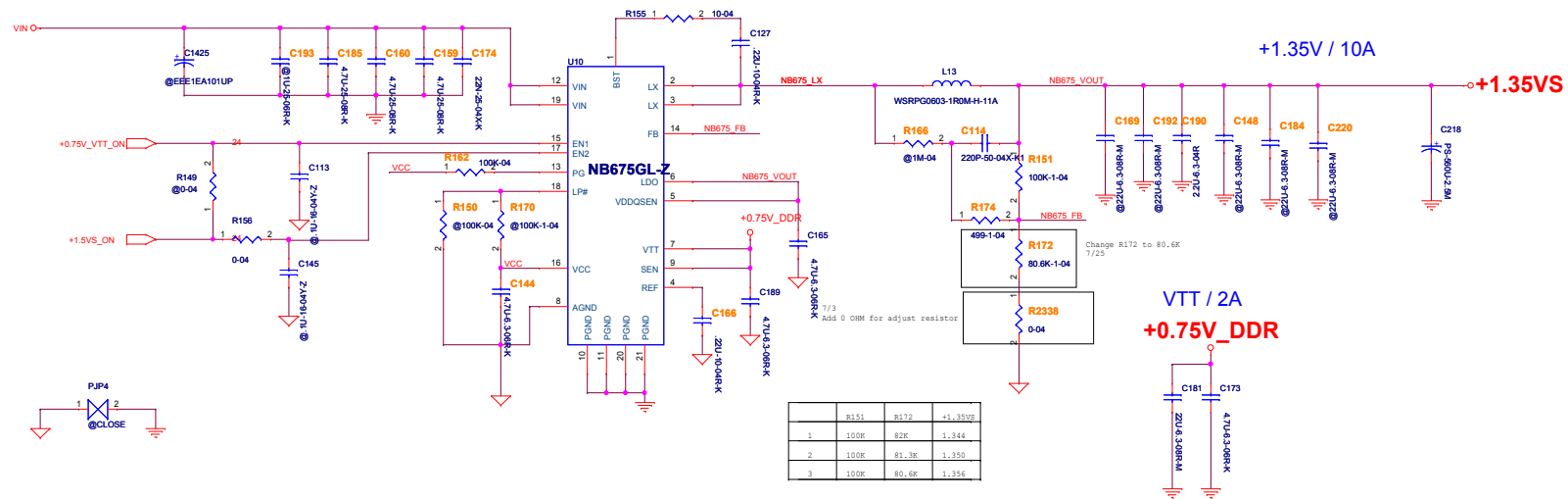
## G SENSOR





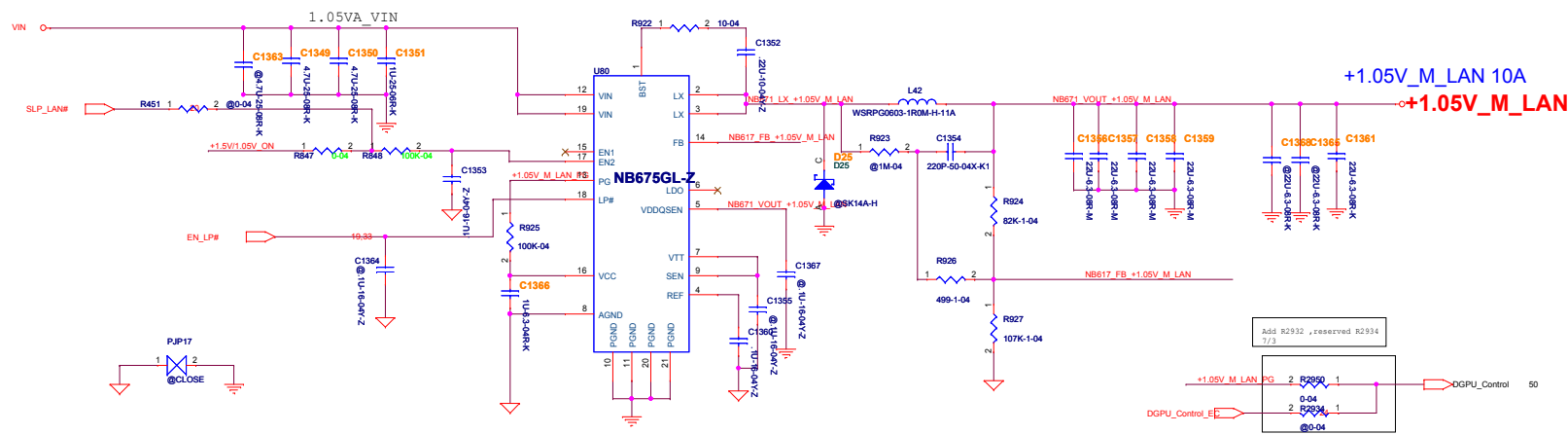
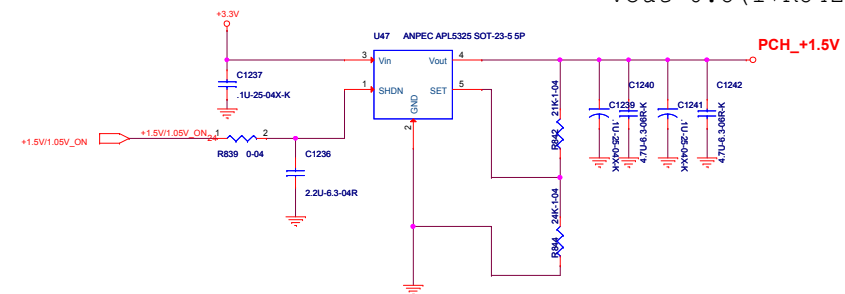


# 1.35VS/VTT Converter



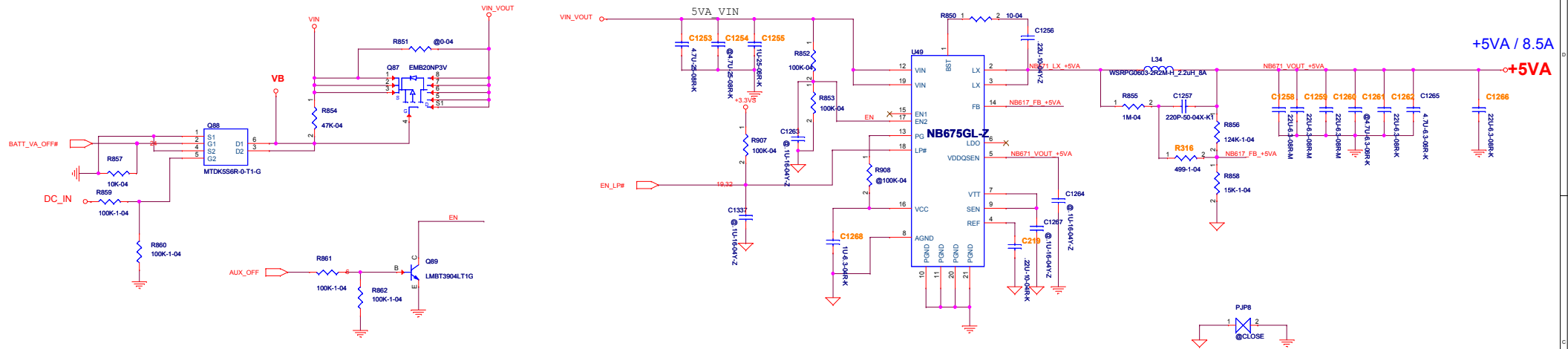
## PCH\_LDO\_+1.5V

$$V_{out} = 0.8(1 + R_{842}/R_{844})$$

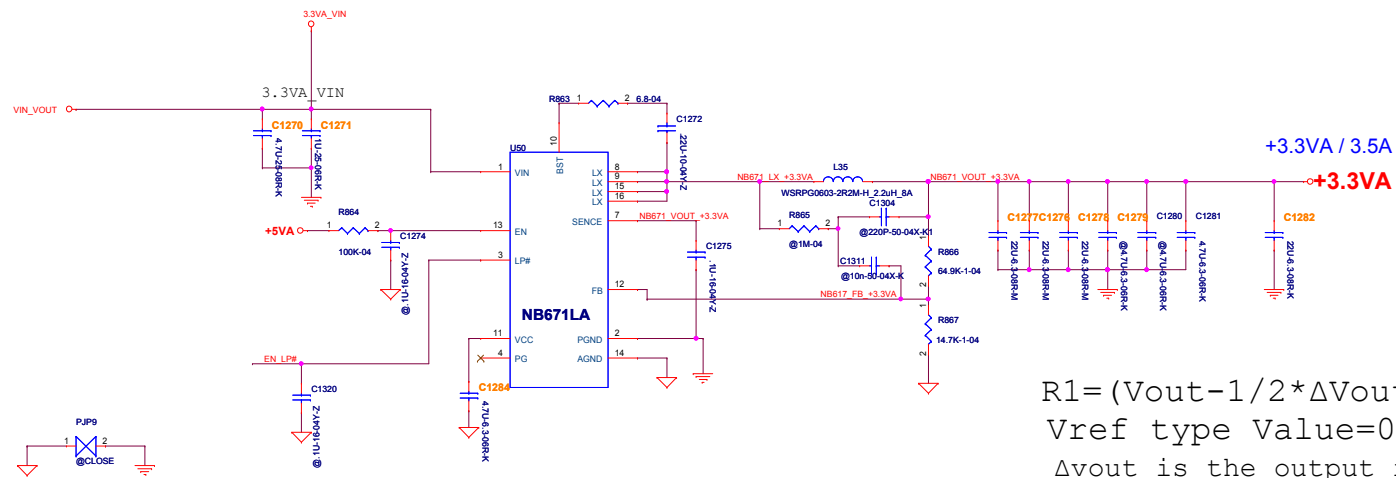




## 5VA Converter



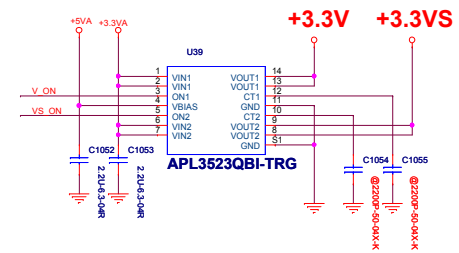
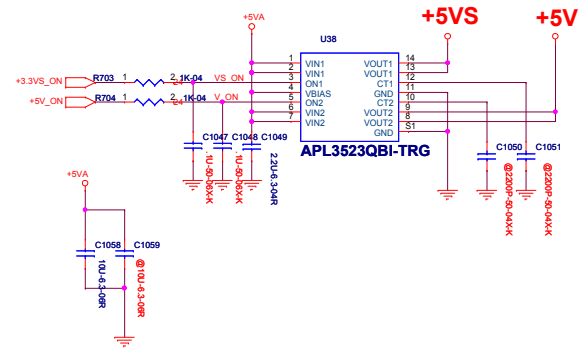
### 3.3VA Converter


$$R1 = (V_{out} - 1/2 \cdot \Delta V_{out} - V_{ref}) / V_{ref} \cdot R2$$

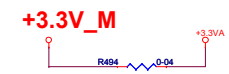
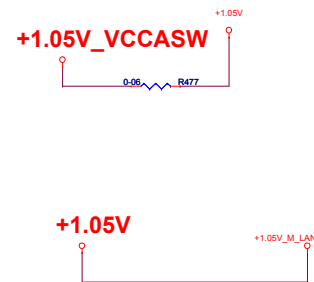
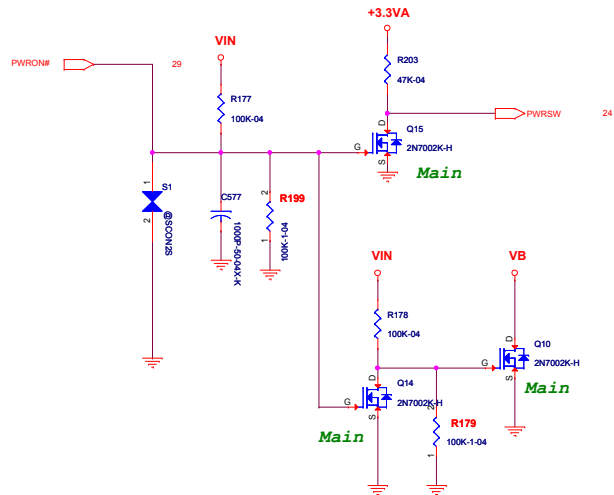
$V_{ref}$  type Value = 0.604 V  
 $\Delta v_{out}$  is the output ripple : 5%  $\cdot V_{out}$







## PWR SW

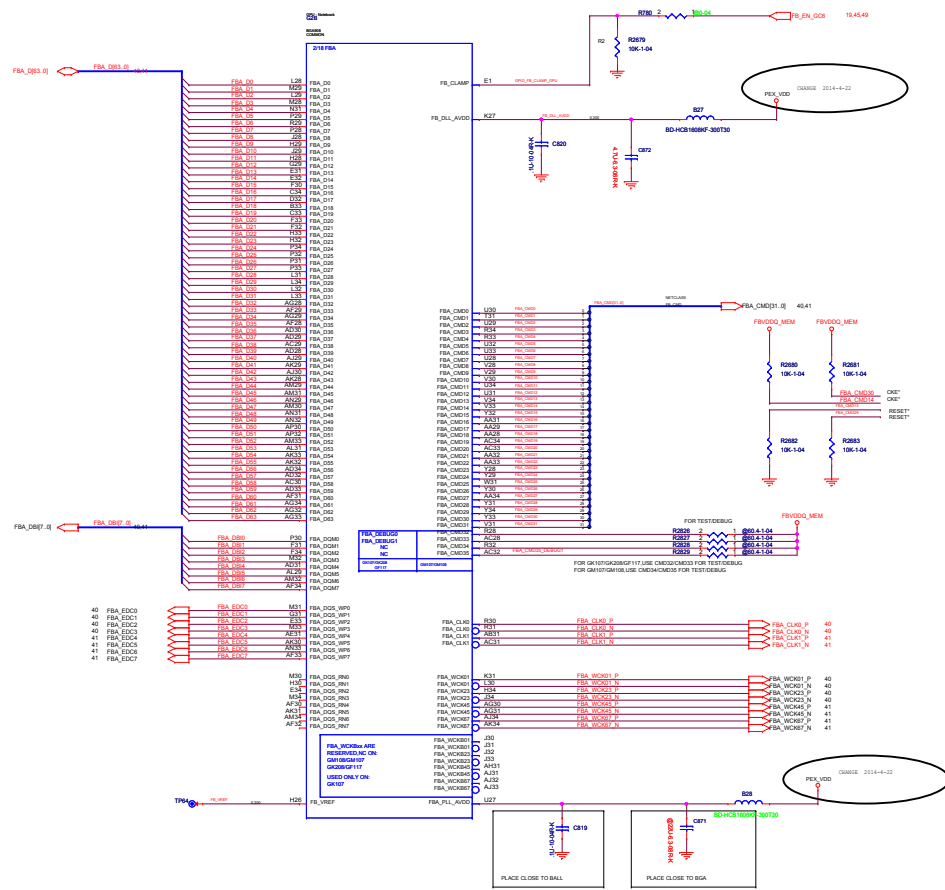


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B	INTEL LAN(82579LM)		RB
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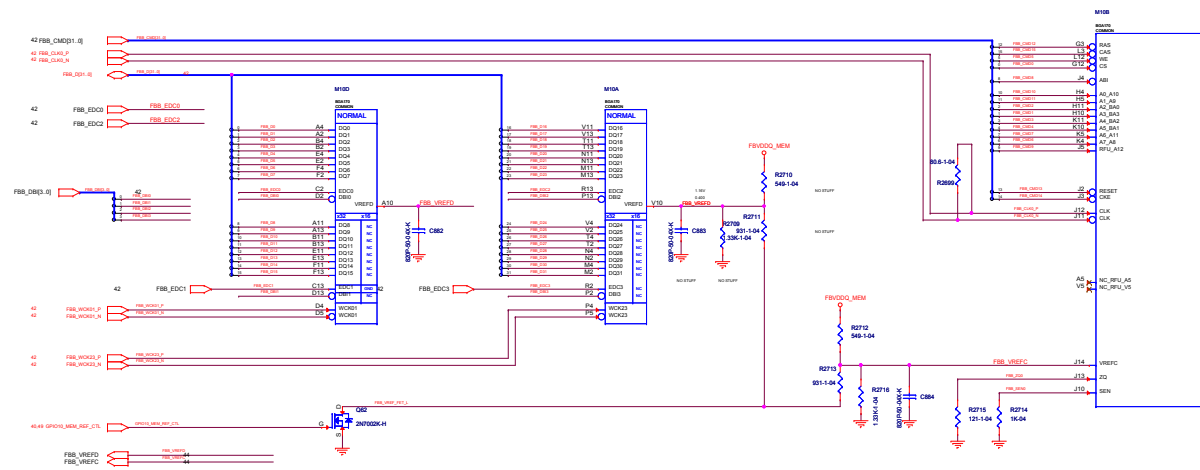




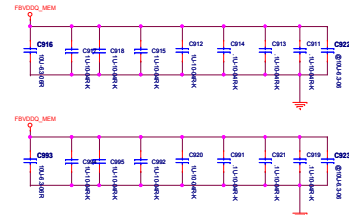
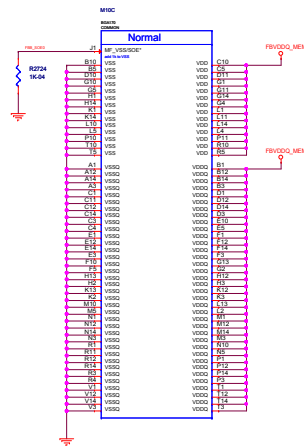




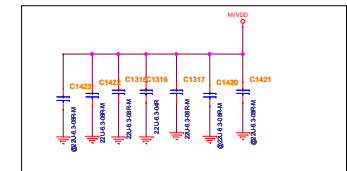




Mirrored: Pull high to VDDQ  
Normal: GND







CR	VREF=2V (Fixed)
>4.5V	Decrease Phase2 current
1.1VCR<1.5V	Remain unchanged
<1.1V	Decrease Phase1 current

```
Iocpsetting=2V/R2846
R2847 is used to set phase current balance
VPhase max=Imax*RDSON/2
```

TC=100 degree  
Q2 ID =49A Q1 ID=29A

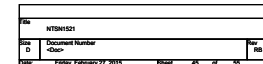
TA=70 degree  
Q2 ID =16A Q1 ID=10.2A

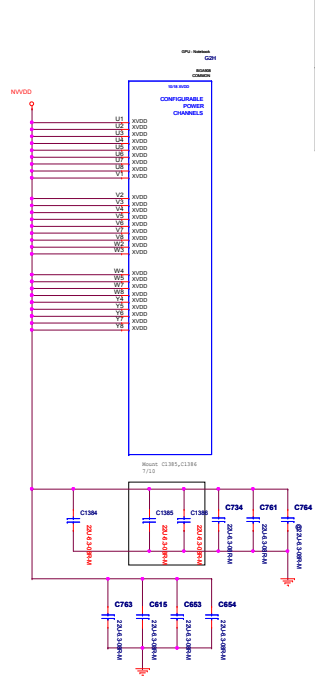
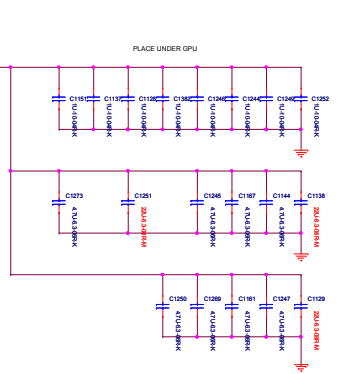
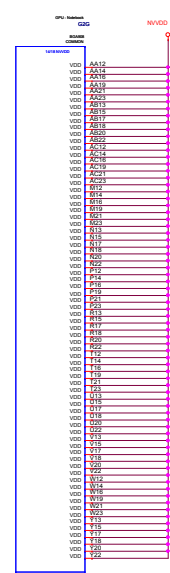
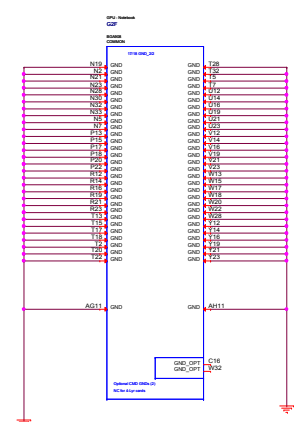
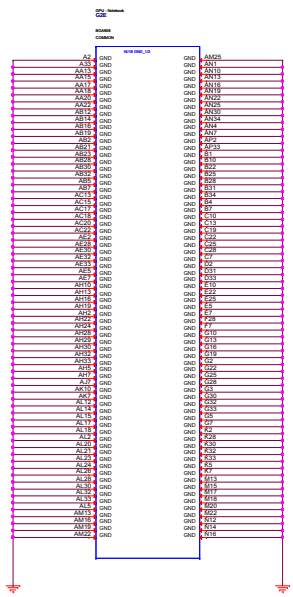
Junction-to-Ambient  
Q2: 51 degree/W Q1: 59 degree/W

Junction to Case  
Q2: 3.4 degree/W Q1: 4.4 degree/W

Package limitation current :Q1=25A,Q2=36A

RDSON  
Q1: 3.3m OHM (78A)  
Q2: 7 m OHM (46A)



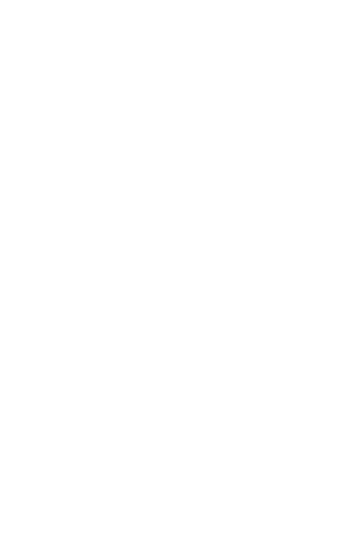
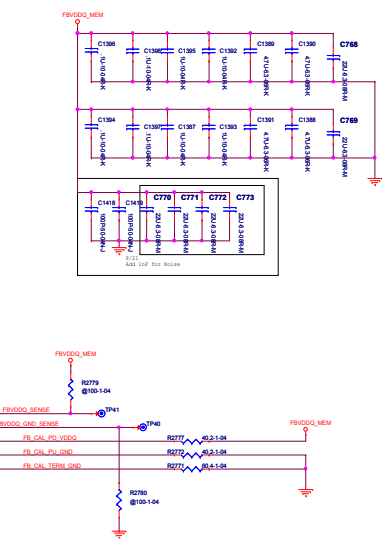
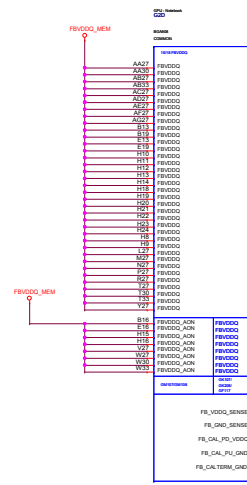


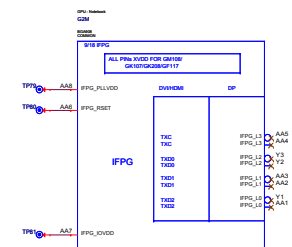
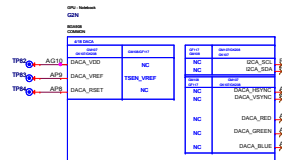
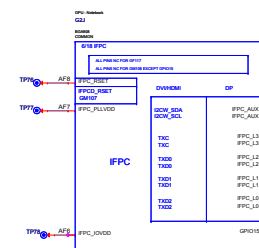
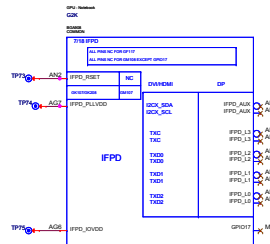
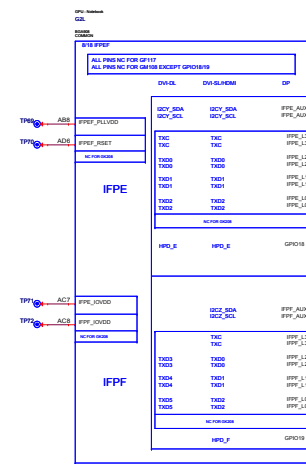
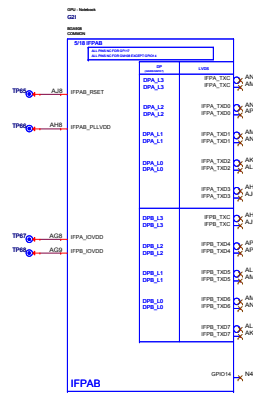
FOR GM107 DECOUPLING CAPS  
UNDER GPU

6X 0005 1uF  
10X 0005 4.7uF  
NEAR GPU  
1X 0005 22uF  
5X 0005 4.7uF  
1X 7705 330uF

FOR GM108 DECOUPLING CAPS  
UNDER GPU

4X 0005 1uF  
10X 0005 4.7uF  
NEAR GPU  
1X 0005 22uF  
1X 0005 4.7uF  
5X 0005 4.7uF  
1X 7705 330uF

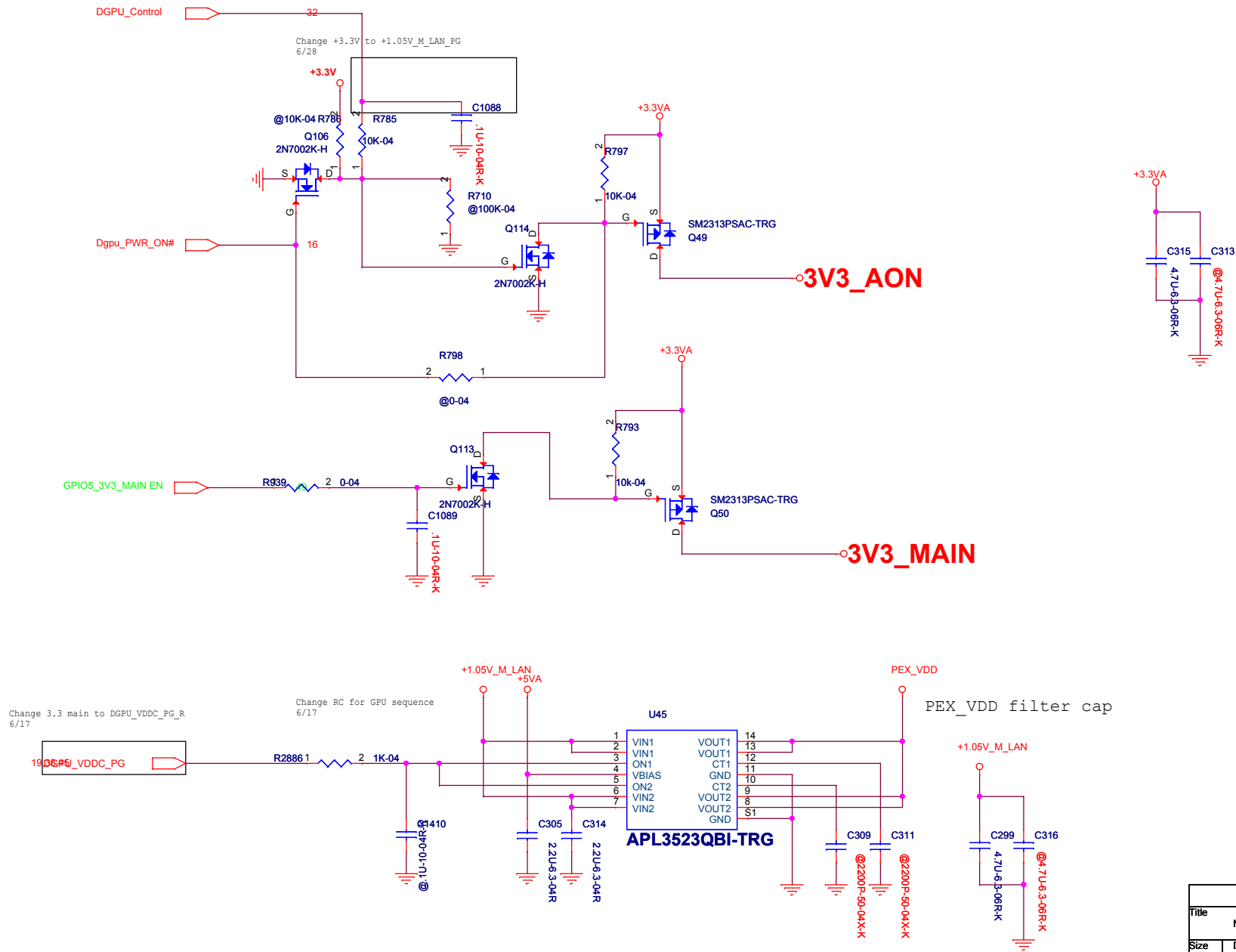






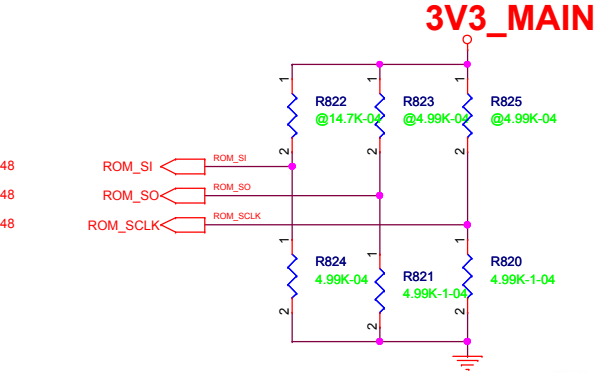






Title		
NTSN1521		
Size	Document Number	Rev
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Date:	Friday, February 27, 2015	Sheet 50 of 55

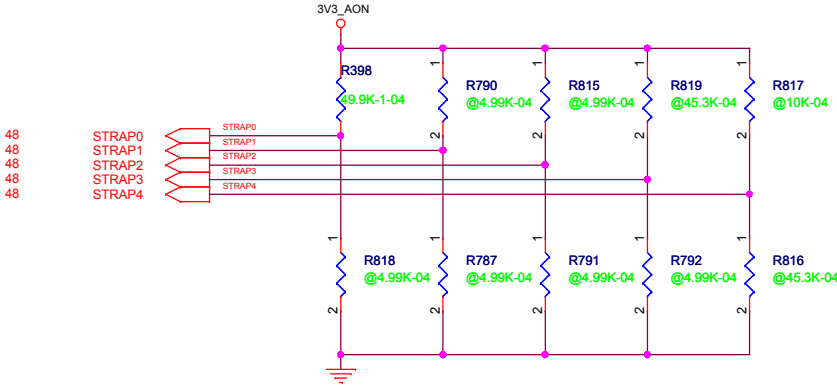
PCI\_DEVID5, PCI\_DEVID4, & SUBVENDOR Strap Selectable



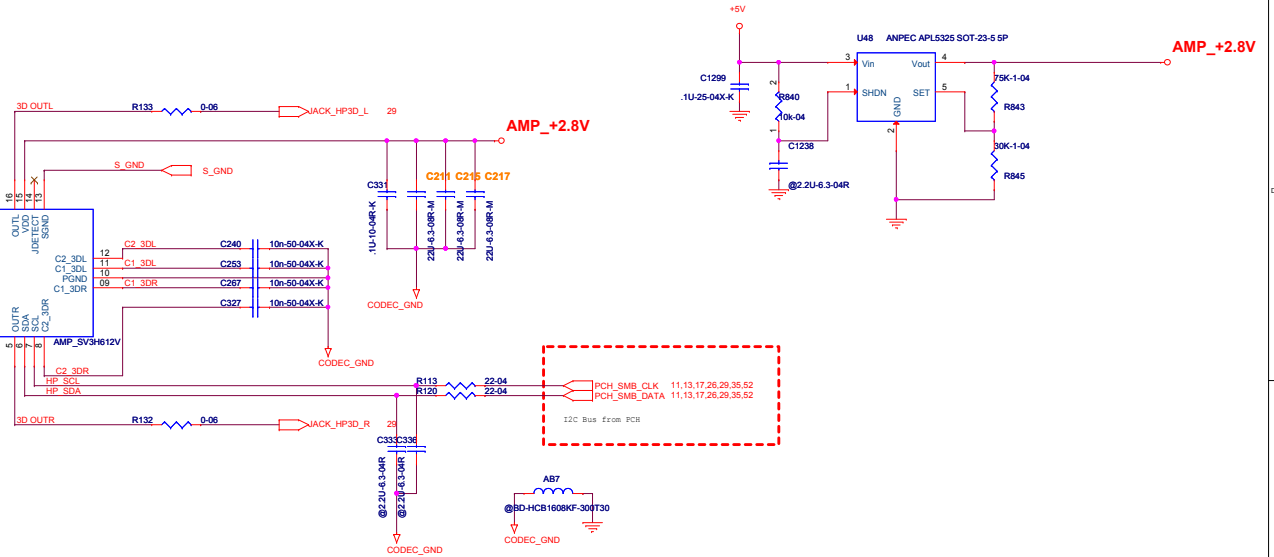
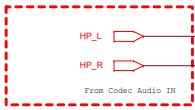
			R824
	Samsung 128MX16	0x0	4.99kohm PULL DOWN
	HYNIX 128MX16	0x1	10kohm PULL DOWN
	MICRON 128MX16	0x5	30.1kohm PULL DOWN
Hynix 2G	HYNIX 128MX32	0x2	15kohm PULL DOWN
Samsung 2G	Samsung 128MX32	0x3	20kohm PULL DOWN
Micron 2G	MICRON 128MX32	0x4	24.9kohm PULL DOWN

Table 11. N15P-GX/GT GDDR5 Recommended Memories

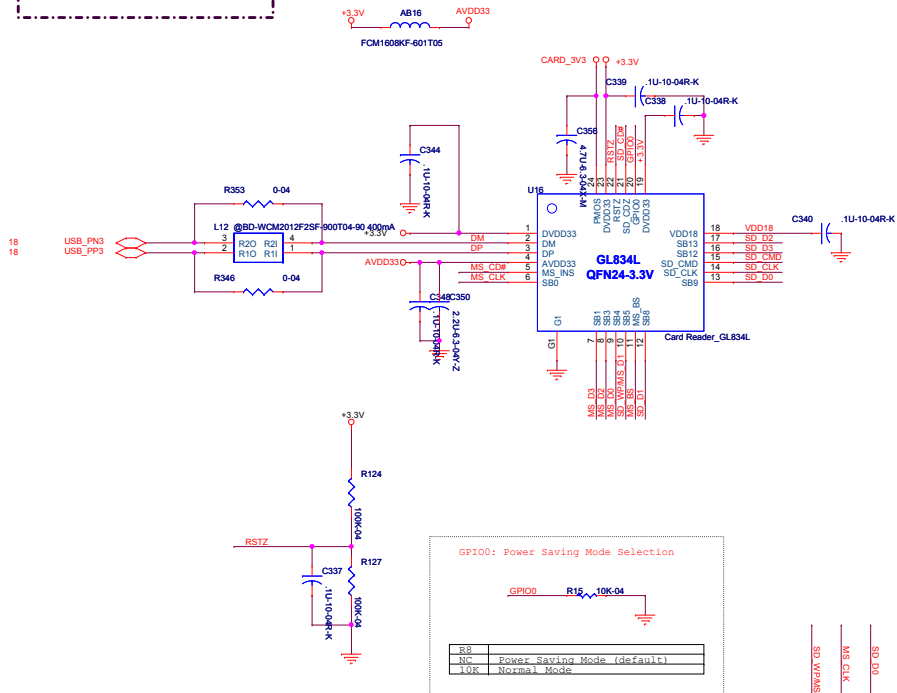
Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V/ 1.35V	128Mx16	Samsung	K4G20325FD-FC03	D-die	0x0	2500	N/A	Production ready
			Hynix	H5GC2H24BFR-T2C	B-die	0x1	2500	1347	Production ready
			Micron	EDW2032BBBG-6A-F	B-die	0x5	2500	N/A	Production ready
		256Mx16	Hynix	H5GC4H24MFR-T2C	A-die	0x2	2500	N/A	Production ready
			Samsung	K4G41325FC-FC03	C-die	0x3	2500	N/A	Production ready
			Micron	EDW4032BABG-60-F	A-die	0x4	2500	N/A	Production ready



SV3H612V  
3D Vol Amp

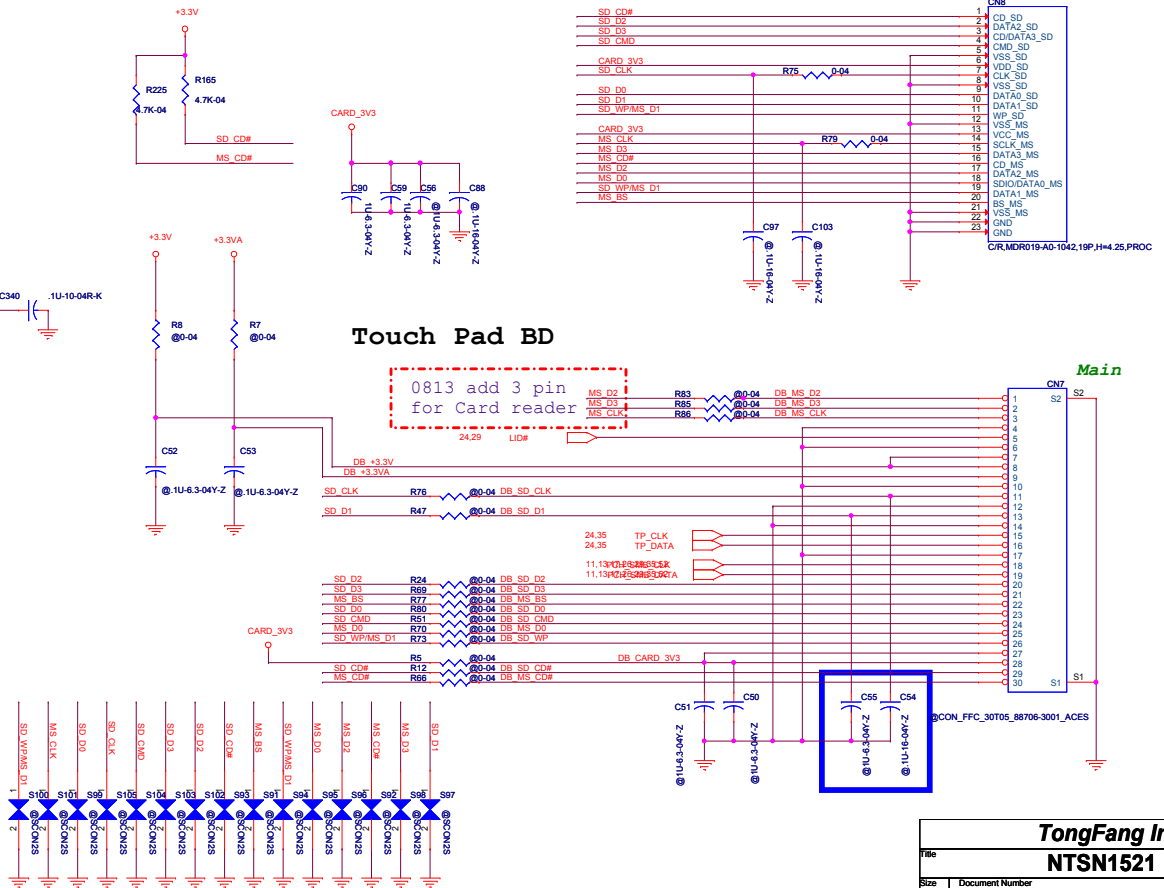


GL834L  
Card reader



Touch Pad BD

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0813 add 3 pin
for Card reader
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Data	Change Content	
5.23	CRT power shares with HDMI power for safety requirement	
5.26	NV requirement 1. Delete GC6_FB_EC. 2.EC send adapter in to GPU	
5.27	NV requirement 1. Delete R706 for removal of GC6_EVENT_EC from EC\ Pin 86. 2. Change Pull high and Pull low for VRAM to match mirror VRAM 3. Mount R333	
5.28	Change KB LED TP LED Side LED supply voltage to 5VS Change R659 to 0 OHM	
5.29	1. Change Value to match footprint C358,C936,937,C419, C1001, C1002,C1376 2. Change R824 to 15K	
6.10	Change R344 to 10 mOHM ,NL_R555,NL_B12,Change R842 to 22K, Mount R13,R508,Change R154 to 20K	
6.12	1.Change R228 to 2.43K, Change R233 to 1.5K, NL C274 for Vcore Power Test issue	
6.17	Change GC6 control GPIO connection and GPU power sequence controlled by GPU_Vcore_PG Change C1309 to 1nF	
6.20	Mount R140, NL R141 for eDP detection	
6.21	Page 6: Mount 6Rs Page11: Mount eDP components and remove RT2136 and add a R for PWM Page 16: Mount R481 Page 24 :R140,R141 Page35: NL Side LED	
6.22	1. Add BAT I schematic ,and delete BAT I Direction	
6.27	1. Reserve PG control circuit (mount D21, NL R396 ) 2. Add EMB dual MOS as 2nd source needing to match OCP resistor	
6.28	1.Change +3.3V to 1.05V_LAN_M_PG(1.Add C1088 2.mount R926 1K C1365) 2. NL R456	
6.30	1. Change R233,R228 C274 for CPU core 2.Add text for Imon explanation	
7.3	1. Add 0 OHM for adjust +1.35, 1.05V 2. Add Boost fan 3. Add 0 OHM for PSI 4. Add 0.1UF*5pcs for EMI 5. Change CPU R228,R233,C274,C285 for TAT 6. NL C243, R555,C1309 7.NL Common choke*1pcs ,Mount 0 OHM *4pcs 8. DMIC : 2pcs resistor, 9. EC control DGPU_ON timing 10. Mount 6pcs cap to CPU Core 11. Add cap to GPU core and VRAM power	
7.4	1.Change U2\vin to 5VA 2. Remove D15 in BAT_I detect circuit 3. Delete Vin AMP,H12 4.Add 0603 CAP to Vcore 5.Reserve POScap to GPU Bottom 6.AC3 PIN2,4 CHANGE NET NAME 7.Change U2 to AZV331	
7.5	1. Mount R27, R28 for mSATA 2. Remove L7 for no Fingerprint 3. Add +3.3Vs on USB board IO for fingerprint 4.Change R337,R319 R value,C274,C258 C value	
7.7	1. Page 6: Add colay R*4 for decreasing eDP signal stub 2. Page 34: correct CN9's SW_BAT pin 3.Add C3209 4.Add Q48 for battery Leakage 5.Update KB pin definition	
7.9	Update Text for VRAM ID R	

Data	Change Content	
7/10	Exchange beep and SenBAT_V for EC pin	
7/14	1. Cancel R3 2.Update EC GPIO according to Ted's mail PID_0_CHG_B_LED (GPA5) SENBAT_V (GPC3) BTL_BEEP (GPA2) 2.Del C1299, mount C1300,C1301 3.Del C182, mount C576,C602	
7/16	Add BAT_I EC table	
7/20	Mount C1291 C1377 C1413 C1193 for GPU Core,VRAM	
7/24	Page 29: Change R2960 to 7.5K Add R2961 ; Change R2933 to 7.5K ; Add R2936 for Boost fan Page 11: Change R913 to 0 OHM, Reserve R932 ,Reserved R506 for eDP panel	
7/25	Change R172, R2906 to 80.6K , R2350 to 44.2K	
8/2	Page 45: Add text for explanation of voltage loop control	
8/5	Page 34: Change RCH2 10 mOHM-->25 mOHM	
8/7	Change RTL8411 to RTL8111G(S) + Card reader	
8/7	add 3D VOL IC SV3H612V	
8/11	add RTL8111G(S) VDD10 Power select circuit	
8/11	colay RTL8111 XTAL to PCH	
8/13	add 3 pin for Card reader	
8/13	USB add colay cap(C1325/C1324 colay with C618 & C619/C614 & C617)	
8/19	PCH +1.5V LDO Change to APL5325	
8/21	Page 35: Add GND to T/P LED	
8/21	Page 46: Add filter cap for VRAM noise :C770 C771 C772 C773 Del: C1283,C1248 change C1138,C1251,C1129 to 22uf Del: C1383, C1381,change C1385,C1384,C1386 to 22uf	
8/21	Page 34: 1. Q48: exchange S and D, 2. Reserve R255, 3. Change SW6 connection Page 45: Del Vin Jumper , Page31: Del Vin Jumper Page 27: Change LED_CR to LED0 for RJ45 LED	
8/21	Page 26: Mount R27 for msATA BD	
8/21	Page 25:R616 , R615 , R608 , R607 , R606 , R605 , R618 , R617: 680-->499 OHM for HDMI Page 34: Change C442's GND to GND for Adaptor_I detector Page11: Not mount CN20	
8/21	Change H14, H15 Footprint	
8/21	Page 34: Add @R257,Reserved for Battery power on Page 41:Change C900,C899, C902 to 22UF Page 40:Change C891,C892,C894 to 22UF Page 32: Colay C1425	
8/21	Page 11:Change B23 to 0805 Fuse,Del C582 Mount C580 Page 24: Add R131	
8/22	page 10: CPU CORE, Del: C671, C682, C665, C677, C683; Add: C1326 poscap. C1307, C1308不上件, C204, C306不上件 page 32:1.35Vs, Add: C218 330uf SMD polymer cap co-lay page 36:Del U23,U24 page 32:+1.05V change NB671 to NB675 page 33:+5VA change NB671 to NB675 page 34:C442 move to the right of R572,add 0.1uf Cap C182 close to EC page 27:Del C268,C330,C224,C326,C325,C223,C256;Add C250	
8/25	Page 27:LED0 add R370	
8/27	Page 29 & 52:SV3H612V change CODEC_GND to S_GND Page 50:3V3_AON change APL3523 to use 4 MOS Page 29:Colay +5V to MIC1_VREF_L Page 32:Del D24	
8/28	Page 29:Add +5V 2 0603cap close to AR23 Page 50:Add Q51	
9/01	Page 52:change C328,C214 to (R133,R132) 0ohm	
9/02	Page 45:C1292 change 1U to 2.7nF Page 46:FBVDDQ_SENSE add 100 ohm pull high;FBVDDQ_GND_SENSE add 100 ohm pull down Page 27:add C252 0.1uF Page 24:LED ON colay with CPPE# Page 48:Modify C1406 to 1uf/0603. Modify C1399 to 22uf/0805. delete R784, VID_PLLVDD can be line to SP_PLLVDD directly. Page 30:reserve 放电电阻for FBVDDQ_SENSE Page 49:GPIOB_STX_FDX_RST_MON#信号预留10K pull up to 3V3_AON Page 48:XTALOUTB信号预留10K pull up. Page 48:STRAP_REF0信号预留10K pull up. Page 45:C1292 change to 2.7nf. Page 46:FBVDDQ_SENSE reserve 100ohm pull up to VDDQ, FBVDDQ_GND_SENSE pull down to GND.	
9/18	Page 48:STRAP_REF0 power change from 3V3_MAIN to 3V3_AON	
9/26	Page 32: 上件R925 Page 52:Del U6 pin13 HP Sensor pin. U16 pin19 connect to +3.3V Page 28:Add Q65,R98,R108 for HP_Sensor	

